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Design of Carry Skip Adder for Reducing Power Consumption

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***Abstract*-A methodology for energy-delay optimization of digital-circuits is presented. This methodology is applied to minimizing the delay of representative carry skip adders under energy constrains and also minimizing the critical path delay to providing high performance, voltage scaling, energy efficient. Carry skip adder (CSKA) structure with AND-OR-Invert (AOI) and OR-AND-Invert (OAI) compound gates are used for the skip logic operation. one of the effective techniques to reduces the power consumption and delay in the digital circuits. The speed is attained by using concatenation and incrementation method. The architectures are designed and implemented by Verilog HDL.**

***Keyword*-Carry skip adder (CSKA), voltage scaling, energy efficient, conventional CSKA (Conv-CSKA),Concatenation and incrementation technique.**

I. INTRODUCTION

In commonly,Adders are very often in the critical path of a computer, so it is very important that their performance will not limit the cycle time of the machine.In very large scale integration (VLSI) applications, area and power are very important factor which must be taken into account in the design of a fast adder. Over the time, the number of transistors on a chip increased exponentially in according with Moor's law. This has controlled to progress in differentiated computing applications, such as health care, security, education, communications etc. Therefore an uncertainty always remains as to whether a high performance or low power could have been achieved in this paper.

Adders are the building block for arithmetic and logic units (ALUS).To upsurge the speed and reducing their power or energy consumption intensely distresses the speed and the power consumption of work stations. Here numerous substance followed to reducing the speed power of here component.

Unique of the proficient methods toward inferior the power consumption of digital circuits to lesser the supply S (potentially) subject to process and environmental deviations access the nanoscale technologies. The requirement of the power (and performance) proceeding the supply voltage consumes be there the inspiration for design of circuits by the feature of energetic voltage and frequency scaling. The supply voltage, one may select among different adder structures/families for optimizing power and speed.

There are many adder families with different delays, power consumptions, and area usages. Examples include ripple carry adder (RCA), carry increment adder (CIA), fast adder (FA), carry skip adder (CSKA), carry select adder (CSLA), and parallel prefix adders (PPAs), Kogge-stone adder, square-root CSLA (SQRT CSLA) adder, variable block adder (VBA),speculative carry select adder (SCSA), cascaded carry-select adder (C^2SA), logarithmic skip adder (LSA), carry lookahead adder (CLA).The RCA can be designed by cascading full adder in serious. This kind of adder is called a ripple carry adder, since each carry bit "ripples" to the next full adder. But it provides large critical path delay, low power and low area.Thekogge-stone adders have large power for the circuits.The CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input and then the final sum and carry are selected by the multiplexers(mux). One

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choice is the carry-skip adder, which because of its great topological regularity and layout simplicity is considered a good compromise in terms of area and performance and low critical path delay.

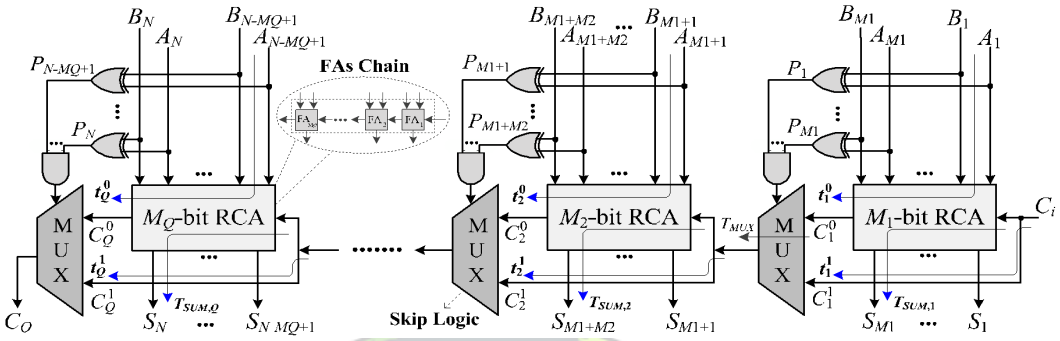

Fig. 1.Conventional structure of the CSKA.

Hereafter, the contributions of this paper can be summarized as follows.

- Recommending a modified CSKA structure by combining the concatenation and the incrementation schemes to the conventional CSKA (Conv-CSKA) structure for enhancing the speed and energy efficiency of the adder. The alteration provides us with the ability to use simpler carry skip logics based on the AOI/OAI compound gates instead of the multiplexer
- Only if a design strategy for constructing an efficient CSKA structure based on analytically expressions presented for the critical path delay. The proposed CSKA to minimize the critical path delay.
- Considering the influence of voltage scaling on the efficiency of the proposed CSKA structure (from the nominal supply voltage to the near-threshold voltage).

The recreation of this paper is prearranged as obeys. Section II converses related work on conventional CSKA structure for cultivating the speed as well as ever- increasing the efficiency of adders at low supply voltages.In Section III,describes the proposedstatic CSKA structure. while Section IVThe results of comparing the characteristics of the structures with those of other adders in simulation level are discussed in Section. Finally, the conclusion is drawn in Section V.

III. CONVENTIONAL CARRY SKIP ADDER

The conventional structure of the CSKA consists of stages containing chain of full adders (FAs) (RCA block) and 2:1 multiplexer (carry skip logic). Christo Ananth et al. [5] proposed a system which contributes the complex parallelism mechanism to protect the information by using Advanced Encryption Standard (AES) Technique. AES is an encryption algorithm which uses 128 bit as a data and generates a secured data. In Encryption, when cipher key is inserted, the plain text is converted into cipher text by using complex parallelism. Similarly, in decryption, the cipher text is converted into original one by removing a cipher key. The complex parallelism technique involves the process of Substitution Byte, Shift Row, Mix Column and Add Round Key. The above four techniques are used to involve the process of shuffling the message. The complex parallelism is highly secured and the information is not broken by any other intruder.
It means that the worst case delay belongs to the case where

$$Pi = Ai \oplus Bi = 1 \quad \text{for } i = 1, \ldots, N$$

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where Pi is the propagation signal related to Ai and Bi .

III.PROPOSED CSKA STRUCTURE

The proposed structure is based on combining the Concantenation and incrementation schemes with the Conv-CSKA structure, and hence, is denoted by CI-CSKA. It provides us with the ability to use simpler carry skip logics. The logic

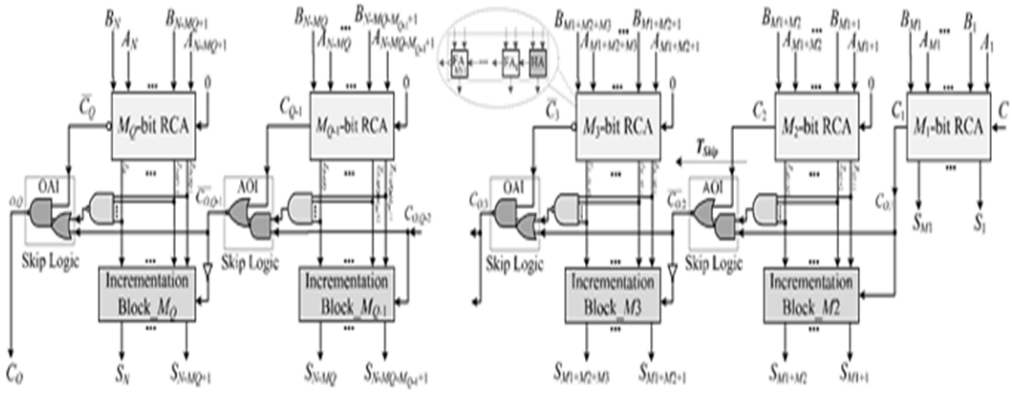

Fig.2.Proposed CSKA structure.

replaces 2:1 multiplexers by AOI/OAI compound gates (Fig. 2). The gates, which consist of fewer transistors, have lower delay, area, and smaller power consumption compared with those of the 2:1 multiplexer. The incrementation block uses the intermediate

results generated by the RCA block and the carry output of the previous stage to calculate the final summation of the stage. The internal structure of the incrementation block, which contains a chain of half-adders (HAs), is shown in Fig. 3.

The reason for using both AOI and OAI compound gates is the skip logics is the inverting functions of these gates in standard cell libraries. This way the need for an inverter gate, which increases the power consumption and delay, is eliminated.This way, since the RCA block of the stage does not need to wait for the carry output of the previous stage, the output carries of the blocks are calculated in parallel.

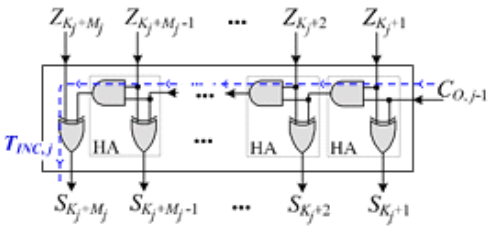

Fig.3. Incrementationblock structure.

IV.CIRCUIT OPERATION AND RESULTS

A.FULL ADDER (FA)

The full adders circuit to the simulation level output is shown in fig.4. Here a, b, c_{in} (carry input) are produced the inputs and sum, c_{out} (carry out) for the adder.

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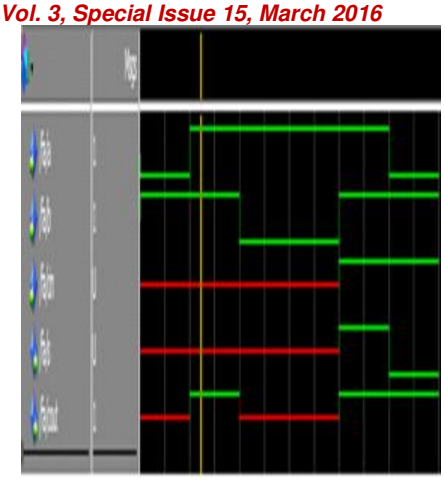

Fig.4.Simulation output for full adders (FAs)

It performs the addition operation for the circuits. The circuits consists of two AND gate, two XOR gate, and one OR gate. Each input have the 8-bit to the function to perform the operation.

B.MULTIPLEXER

The multiplexer circuit perform the 2^n input to the output one output ie. $(2^n:1)$.

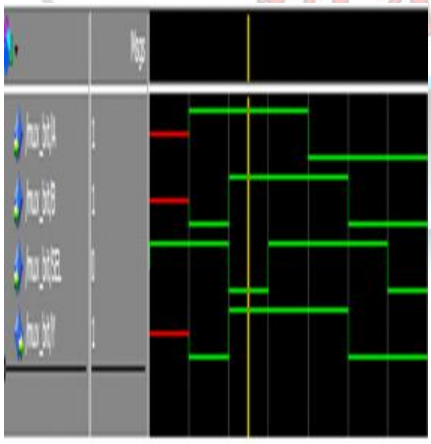

Fig.5. Simulation output for multiplexer

The results suggested the CI-CSKA structure as a very good adder for the applications where both the speed and energy consumption are critical .

C.CSKA

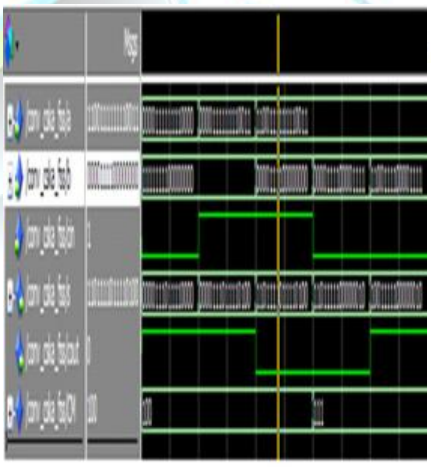

Fig.5. Simulation output for CSKA

The simulated output values for CSKA is shown in above fig. i.e it shows the

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carry skip logic by using AOI nad OAI compound gates.

VII. CONCLUSION

During this paper, a static CMOS CSKA structure called CI-CSKA was anticipated, which exhibits a higher speed and lower energy consumption compared with those of the conventional one . The speed enhancement was achieved by modifying the structure through the concatenation and incrementation techniques. Inaddition, AOI and OAI compound gates were exploited for the carry skip logic .

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