ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 3, Special Issue 15, March 2016

Design of DADDA Multiplier for Image Applications

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Abstract- **Fast arithmetic circuit designing is the key element to the computing systems with high-performance. Particularly Multiplication is a heavily used arithmetic operation that figures Multiplication is a frequently used arithmetic operation that figures certainly in signal processing and scientific applications. Multiplication is hardware intensive, and the main proof of interest is higher speed, lower cost, and less VLSI area. By comparing the multipliers, dadda multiplier has a specified steps to reduce the parameters, which having three multiplication steps for partial product reduction. The approximate compressor for dadda multiplier has been designed using two different new approximate 4-2 compressor designs. Image multiplication is a growing factor in real time applications. By using this multiplier the application of image multiplication is proposed with the help of Xilinx and MATLAB.**

Key words: dadda multiplier, image processing, MATLAB, Xilinx, VLSI.

1. INTRODUCTION

Adders and multipliers have been plays a vital role in the designing of computer arithmetic circuits. Multipliers consume more power, occupy large area and will take more operating time. The performance of multipliers helps to determination of processor's speed and performance of many DSP algorithms. Because of these reasons, the designers are focusing on multipliers of high speed with low power delay product. Delay, area and power consumption have become the paramount concerns in designing of computing systems. By Moore's law speed and dense of transistor in integrated circuits have increased exponentially. The concept is accepted that this exponential increment trend will be end because it is not clear exactly how dense and fast IC'S will reached this point. Power has become the most important concern in designing, not only for the functionality on a chip, but also for density and computing power of integrated circuits. With the increased need of high speed and low power VLSI devices, there is a continuous demand for high speed multipliers.

Low power consumption is also an important concern in design of multiplier. To reduce significant power consumption through reduce the number of operation through reducing dynamic power which is a main part of total power consumption so the need of high speed and low power multipliers have increased. Designers mainly concentrate on only high speed and low power efficient circuit design. The objective of a good multiplier is to provide a physically packed together, high speed and low power consumption unit. Different types of multipliers are Booth multiplier, Sequential multiplier and combinational multiplier, Wallace tree multiplier.

A digital image is an arrangement of picture elements, of ones and zeros. The processing of images is faster and more cost-effective. Image multiplication comes in two main forms. The first form takes two input images and produces an output image in which the pixel values are just combination of the first image, multiplied by the values of the corresponding values in the second image. The second type takes a single input image and produces output in which each pixel value is multiplied by a specified constant. This final form is probably the more extensively used and is generally called *scaling*.

Approximate Multiplier

A novel approximate multiplier design is constructed using a simple, yet fast approximate adder. This newly designed adder can process data in parallel by cutting the carry propagation chain (and thus, introducing an error). It has a critical path delay that is even shorter than a conventional one-bit full adder. Albeit having a high error rate,

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this adder simultaneously computes the sum and generates an error signal;

This feature is employed to reduce the error in the final result of the multiplier. In the proposed approximate multiplier, a simple tree of the approximate adders is used for partial product accumulation and the error signals are used to compensate the error for obtaining a better accuracy. Compared to the traditional (exact) Wallace and Dadda trees, the proposed multiplier has a significantly shorter critical path as well as a reduced circuit complexity.

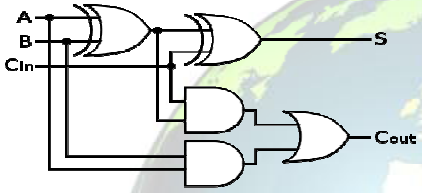

Fig.1 An exact full adder circuit

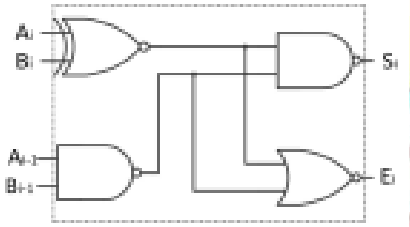

Fig.2 Approximate full adder circuit

3. Two Designs of Multipliers

The design of approximate compressor to be utilized in approximate multiplier is designed in two different methods. Two designs of an approximate compressor are completed. Probably to design an approximate 4-2 compressor, exact full-adder cells are replaced by an approximate full-adder cell.

Design 1:

In the design1 approximation, we approximate the result by making Carry'=Cin with this approximation the carry output in an exact compressor has the same value of input Cin. In particular, the simplification of sum to a value of 0 reduces the difference between the approximate and the exact outputs as well as the complexity of its design. Also, the presence of some errors in the sum signal will results in a reductions of the delay of producing the approximate sum and the overall delay of the design.

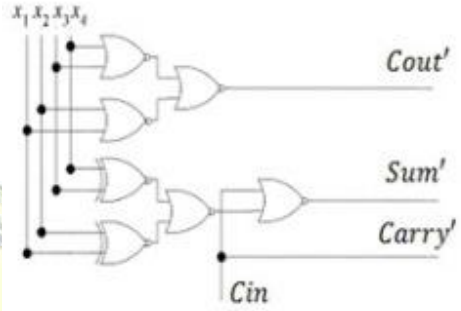

Fig.3 Gate Level Design of design1

$$C_{out}' = \overline{(\overline{x1x2} + \overline{x3x4})}$$

$$Sum' = C_{in}'(\overline{x1 \oplus x2} + \overline{x3 \oplus x4})$$

It is the same as for the exact compressor. However, the propagation delay through the gates of this design is lower than the one for the exact compressor.

Design 2:

A second design of an approximate compressor is proposed to further increase performance as well as reducing the error rate. Since the carry and cout outputs have the same weight, the proposed equations for the approximate carry and cout in the previous part can be interchanged.

$$Sum' = (\overline{x1 \oplus x2} + \overline{x3 \oplus x4})$$

$$C_{out}' = \overline{(\overline{x1x2} + \overline{x3x4})}$$

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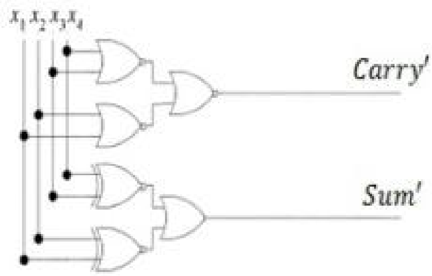


Fig.4 Gate Level Design of design2

The delay of the critical path of this approximate design is 2D, so it is 1D less than the previous designs; moreover, a further reduction in the number of gates is accomplished.

4. APPLICATIONS OF APPROXIMATE MULTIPLIER

Multipliers have been used in various applications in today's life.

Binary Multiplication

Binary multiplication uses the same algorithm, but uses just three order-independent facts: 0 x 0 = 0, 1 x 0 = 0, and 1 x 1 = 1 (these work the same as in decimal). If you perform the multiplication phase with these facts, notice two things: there are never any carries, and the partial products will either be zeros or a shifted copy of the multiplicand.

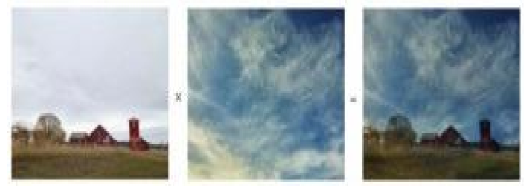
```
     1011.01
  x    110.1
  ----------
      101101
           0
    101101
   101101
 -----------
 1001001.001
```

Fig.5 Binary multiplication

Image Multiplication:

In this image multiplication applications input images and output images both are having pixels corresponding to where they are used. Multiplying the pixels of two input images will provide the output image. For example, images are given below,

(a)



(b)

Fig.6 (a) (b) examples for image multiplication

Image multiplication using MAT lab &Xilinx

The proposed design is designed using Verilog HDL and simulated using MATLAB and Modelsim. The input to the Verilog is in the form of text/pixel values. The edges of an image are determined by comparing the neighbouring text pixels. The edge detected output is in the form of text/pixel values. MATLAB is used for the conversion of the input image to text/pixel values and output edge detected text/pixel output to the edged output. The proposed design can be implemented for any format of images like jpg, gif, bmp etc. Christo Ananth et al. [4] proposed a system in which the complex parallelism technique is used to involve the processing of Substitution Byte, Shift Row, Mix Column and Add Round Key. Using S- Box complex parallelism, the original text is converted into cipher text. From that, we have achieved a 96% energy efficiency in Complex Parallelism Encryption technique and recovering the delay 232 ns. The complex parallelism that merge with parallel mix column and the one task one processor techniques are used. In future, Complex Parallelism single loop technique is used for recovering the original message.

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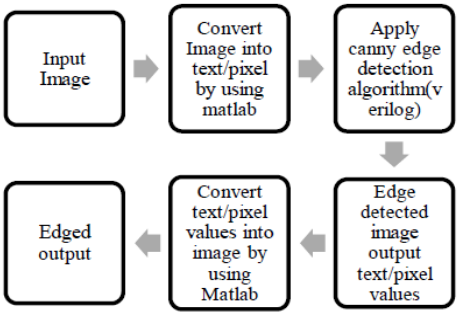

Fig.7 Conversion of image to text file

Conversion of input image to text/pixel values

First consider input image, it is given as input to MATLAB; image is converted in to RGB to GRAY scale image then the image is resized. The identical pixel values are removed from the resized image, which means that the useless information is removed from the resized image which is called as Reshaped image; the reshapes image is then digitalizes in which the input image is converted to the text/pixel values.

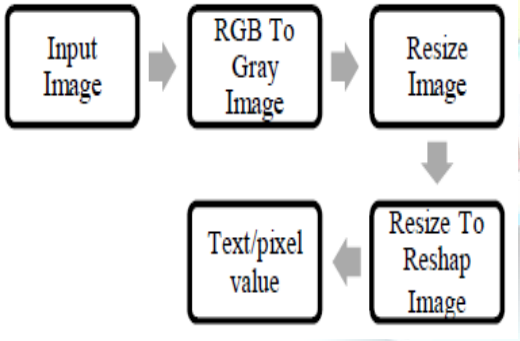

Fig.8 Input image converted to image/pixel using MATLAB

5. SIMULATION AND RESULTS

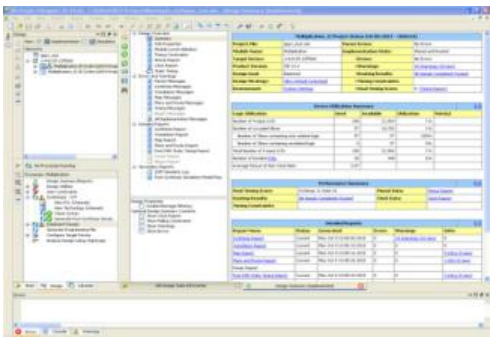

Fig.9 Synthesis Report of Multiplier 1

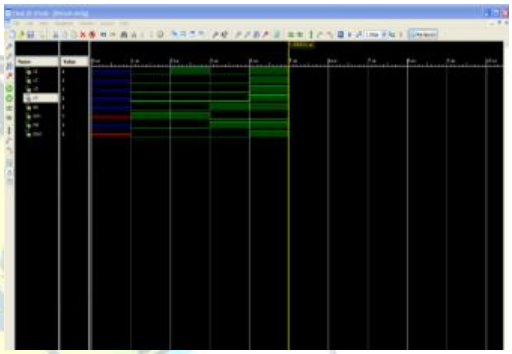

Fig.10 simulation of approximate compressor design 1

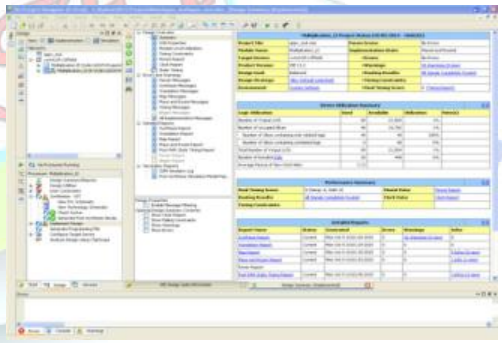

Fig.11 Synthesis Report of Multiplier 2

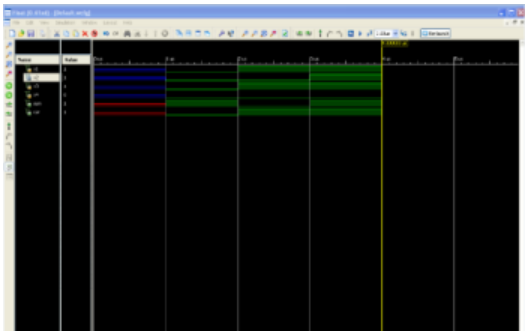

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Fig.12 Simulation of approximate compressor design 2

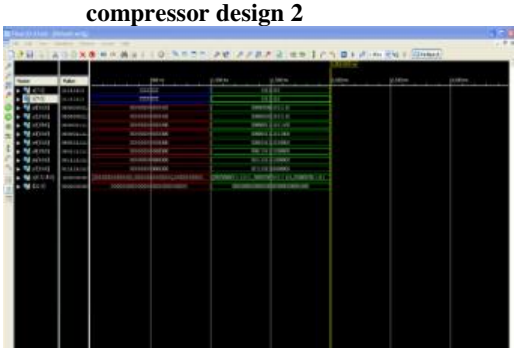

Fig.13 Simulation of Partial Product Generation

6. CONCLUSION

In this paper, 8x8 bit approximate multipliers are designed using 4-2 compressors using approximate full adders. Simulation results have been implemented reported. These approximate compressors are designed using XOR-XNOR based full adders and two modules of multipliers are designed. And finally concluded that the second design of multiplier using full adders have significant reduction in parameters and which is suitable for implement the multiplication with low power and reduced area. The application of image multiplication is proposed and implemented using MATLAB and Xilinx software.

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