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Comparative Analysis: Self-timed Adder Topologies using Different Approaches

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Abstract: **As technology scales down into the less nanometer values power, delay, area and frequency becomes important parameters for the analysis and design of any circuits. In this paper, an asynchronous parallel self timed adder based on a recursive formulation for performing multi bit binary addition is being implemented for various mobile applications and a technique named as radix approach have been applied for the same design for further reduction in power consumption, delay, transistor count. This technique is used to compare with conventional adder. For bits that do not need any carry chain propagation the operation is parallel. The carry look ahead technique is used for reducing carry. For the purpose of comparative analysis of two different approaches based 8-bit different adder Design using 180nm technology, we use TANNER tool.**

Keywords: Binary addition, Recursive formulation, Radix approach, Carry Look-ahead adder.

I.INTRODUCTION

The adder is the most commonly used arithmetic block of the Central Processing Unit (CPU) and Digital Signal Processing (DSP), therefore its performance and power optimization is of utmost importance. With the technology scaling to deep sub-micron, the speed of the circuit increases rapidly. At the same time, the power consumption per chip also increases significantly due to the increasing density of the chip. Therefore, in realizing modern Very Large Scale Integration (VLSI) circuits, low-power and high-speed are the two predominant factors which need to be considered. Like any other circuits' design, the design of high-performance and low power adders can be addressed at different levels, such as architecture, logic style, layout, and the process technology. As the result, there always exists a trade-off between the design parameters such as speed, power consumption, and area. The objective of our paper is to design a lower-power and smaller area as a prime consideration.

Adders are considered to be the heart of computational circuits and addition has been the core for many complex arithmetic circuits. Thus enabling the researcher's to use addition for lot of mobile applications. Processors perform addition as the most important operation. Most of the adders have been designed for asynchronous circuits as asynchronous circuits do not assume any quantization of time and some still use synchronous circuits as well. Thus, addition operation is free from various problems of clocked (synchronous) circuits. Here we have generated the design of binary adders and concentrated on asynchronous self-timed adders.

Self-timed points to logic circuits that depend on or engineer timing assumptions for the correct operation. These Self-timed adders have the capacity to run faster than the conventional circuit design. This paper presents an asynchronous parallel self-timed adder (PASTA). This design uses half-adders (HAs) along with multiplexers requiring minimal interconnections. Thus, it is making way for many VLSI implementations. For independent carry chain blocks PASTA works in a parallel manner. There are four levels of minimization of power dissipation in CMOS based system designs: technology, circuit, architecture and algorithm. Generally choosing appropriate algorithm design style 20% to 30 % power can be saved in circuit level. When handling with the rising challenges of digital circuit's design the Radix approach is superior.

An asynchronous parallel adder using a radix Full Adder (FA) is presented here. The basis of the design of this adder is a 24-bit transistor mirror FA. Therefore, it is feasible for VLSI implementation. To obtain an efficient area implementation, the carry is first generated on its critical path and reused in sum generation. For speed optimization, two full adders are joined for a radix-4 FA block. To shorten the carry path carry look ahead technique has been used

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This paper is organized as follows. In Section 2, we the different adder architectures are reviewed. Section 3 explains the performance of PASTA. In Section 4, transistor mirror and radix FA is discussed. Final result is discussed in Section 5 and the conclusions are summarized in Section 6.

II. BACKGROUND

Self-timed circuit which is a sequential digital logic circuit is not controlled by global clock signal or clock circuit but they often use signals that depict the completion of operation and instructions. They can be classified into two types:

A. Pipelined adders using single-rail data encoding

To enable the adder block as well as to establish the flow of carry signals the asynchronous Req/Ack handshake can be used. These representation of dual-rail signal can be done in more than two logic values (invalid, 0, 1), and thus when a bit operation is completed it can be used to generate bit-level acknowledgment. When all bit Ack signals are received (high) final completion is sensed.

B. Delay insensitive adders using dual-rail encoding

Asynchronous adders that assert bundling constraints or DI operations are Delay Insensitive (DI) adders. Thus, in presence of bounded but unknown gate and wire delays they can correctly operate. Some of the types of DI adders, such as DI ripple carry adder (DIRCA) and DI carry look-ahead adder (DICLA). Dual-rail encoding and are assumed to increase complexity which are used in DI adders. Using dynamic logic or only nMOS designs dual-rail encoding can still be used to produce circuits as efficient as that of the single-rail variants though it doubles the wire complexity. One example where 40 transistors per bit is used in DIRCA adder while the conventional CMOS RCA uses only 28 transistors making drastic reduction in transistor count. Some design techniques for digital integrated circuit are as below:

1. CMOS design technique:

Most of logic gates in VLSI use standard CMOS circuits with complementary pMOS pull-up networks and nMOS pull-down design. This is because they have low power insensitive to device variations, good noise margin, fast and can be easily designed using any of the tools one among is Cadence. The AC power caused by the charge and discharge of capacitances helps in determining the power consumption of conventional CMOS circuit:

$$\text{Power} = CV2f \text{ ---- (1)}$$

Where f is the frequency at which the capacitance charges and discharges. The frequency goes up as does the power consumption when the circuits get faster.

2. Pass Transistor Logic:

To reduce the number of transistor required to implement logic an alternative to complementary CMOS is pass transistor logic, which allows the primary inputs to drive source drain terminal and also gate terminal. Christo Ananth et al. [3] proposed a system which can achieve a higher throughput and higher energy efficiency. The S-BOX is designed by using Advanced Encryption Standard (AES). The AES is a symmetric key standard for encryption and decryption of blocks of data. In encryption, the AES accepts a plaintext input, which is limited to 128 bits, and a key that can be specified to be 128 bits to generate the Cipher text. In decryption, the cipher text is converted to original one. By using this AES technique the original text is highly secured and the information is not broken by the intruder. From that, the design of S-BOX is used to protect the message and also achieve a high throughput, high energy efficiency and occupy less area. Also reduced number of transistors and lower interconnection effects are obtained due to low power dissipation.

3. Dual pass transistor technique:

This has twice as the number of transistors as CPL for any particular function. Covering every input vector in the Karnaugh map twice is the logic behind the design of DPL. The design of parallel self-timed adder is carried out using all these above techniques to check for the variation in the efficiency. But the disadvantage of this design is the number of transistor. This paper implements a new low power design technique that solves most of the problems in above digital design. Using only two transistors GDI approach allows implementation of a various logic functions. For design of fast, low

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power circuits with less number of transistors this method is best suited.

4. GDI technique:

The basic GDI cell is a conventional CMOS inverter, but there are some modifications made they are: i) the three inputs of GDI cell are: P (input to the source/drain of pMOS), G (common gate input of nMOS and pMOS) and N (input to the source/drain of nMOS). ii) In comparison with a conventional CMOS inverter bulks of both nMOS and pMOS are connected to N or P (respectively) and can be biased. Those functions which cannot be implemented using standard p-well CMOS process can be successfully implemented in twin-well CMOS or silicon on insulator (SOI) technologies. The most complex design that can be implemented with GDI is the MUX design. Traditional CMOS or PTL design requires 8-12 transistors unlike GDI design which requires 2 transistors only.

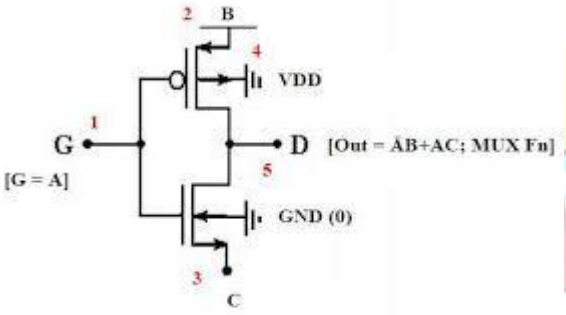

Fig. 1 Basic GDI cell

The disadvantage of GDI is that of reduced swing, i.e., degraded output depending on the combination of the each input.

III. Design of PASTA

The architecture and theory of PASTA is explained. This adder initially accepts two input operands to perform half adder additions for every bit. Later it keeps iterating using previously generated sums and carry to perform half adder additions continuously till where all carry bits are at zero level.

A. Architecture of PASTA

The architecture of the PASTA adder is shown in Fig. 2. The Req handshake signal is corresponded to selection input for two input multiplexers and will be a single 1 to 0 transition denoted by SEL. Initially it will select the actual operands 'a' and 'b' during SEL = 0 and when SEL = 1 it will switch to feedback/carry paths for subsequent iterations. Multiple iterations are enabled by feedback path from the HAs which continues till the completion of all carry signals to assume zero value.

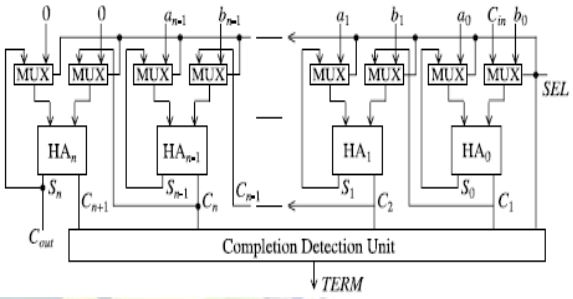

Fig. 2 Architecture of PASTA

B. State Diagrams

We have Fig. 3 which depicts the two state diagrams for initial phase and then iterative phase of the above architecture. Each state is depicted by (Ci+1 Si) pair where Si, Ci+1 represent carry out and sum values respectively, considering the ith bit adder block. During the iterative phase i.e. when (SEL = 1), the feedback path through multiplexer block is activated. To complete the recursion the carry transitions (Ci) is generated various times as needed. During the initial phase, the circuit works as a combinational HA. State (11) cannot appear because of the use of HAs instead of FAs.

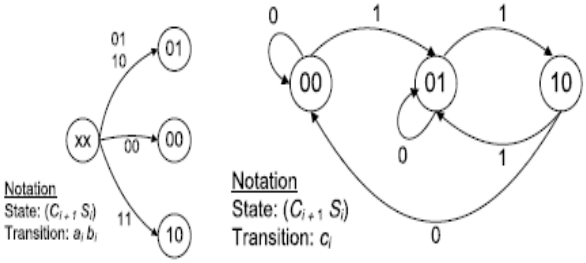

Fig. 3 Two states of PASTA

C. Recursive Formula for Binary Addition

Let us consider S ji and C ji+1 as sum and carry respectively, at the j th iteration for ith bit. The initial

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condition (j = 0) for half adder addition is obtained as below:

$$S0i = ai \oplus bi$$
$$C0i+1 = ai\ bi. \quad (1)$$

For the recursive addition the j th iteration is obtained by

$$S\,ji = S\,j-1 \oplus C\,j-1i,\ 0 \le i < n \quad (2)$$
$$C\,ji+1 = S\,j-1i\ C\,j-1i,\ 0 \le i \le n. \quad (3)$$

At kth iteration the recursion is terminated i.e. when the below condition is satisfied:

$$Ckn + Ckn-1 + \cdots + Ck1 = 0,\ 0 \le k \le n. \quad (4)$$

D. Drawbacks

When SEL =1, the feedback path from the HAs enables the several iterations and it continue till the completion when all carry signals will assume zero values. Due to multiple iterations, the delay gets increased and the speed of operation is slow. Hence the adder consumes more power and generates high fan-in problems.

IV. IMPLEMENTATION

For the recursive circuit conventional CMOS implementation is depicted in Fig. 4. We have used cadence virtuoso for implementing multiplexers and HA blocks. The SEL will be negated when considering completion detection unit to generate an active high completion signal (TERM). A practical alternative pseudo-nMOS ratio-ed design requiring a large fan-in n-input NOR gate. As all the connections are in parallel the completion detection unit avoids the high fan-in problem. To VDD of this ratio-ed design the pMOS transistor is connected when few nMOS transistors are on simultaneously resulting in static current drain. The negative of SEL signal is also included for the TERM signal in addition to the Ci s, to ensure that during the initial selection phase of the actual inputs the completion cannot be accidentally turned on and in turn preventing the pMOS pull up transistor from being always on.

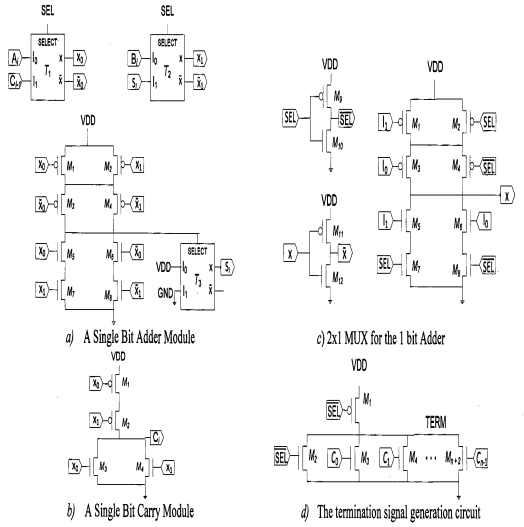

Fig. 4 (a) Single-bit sum module. (b) 2×1 MUX for the 1 bit adder. (c) Single-bit carry module. (d) Completion signal detection circuit.

V. PROPOSED METHOD

A. 24-Bit Transistor Mirror FA

A popular topology is the mirror FA, which contains a maximum of two series transistors, can be observed in the carry-generation circuitry and it is used as the base topology for our designs. The carry is generated first considering it is on the critical path, and then it is used in the sum generation to achieve low area. Mirror FA that consists of 24 transistors is shown in Fig 5. FAs implement the Boolean function, which is given in following equation

$$C_{out} = (A+B)C_{in} + A.B$$
$$Sum = \overline{C_{out}}.A + \overline{C_{out}}.B + \overline{C_{out}}.C_{in} + A.B.C_{in}$$

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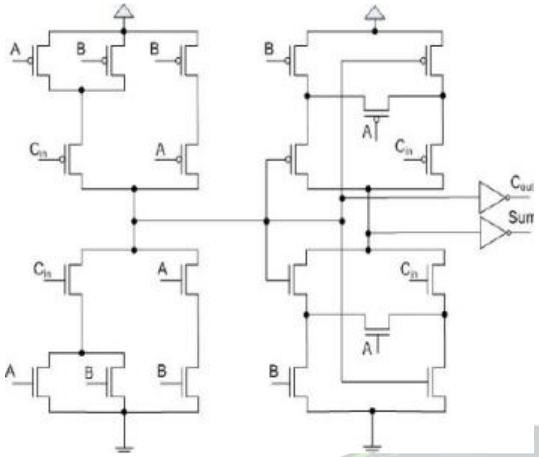

Fig 5: 24-Bit Transistor Mirror FA

B. Basic Radix-4 FA

The main objective in this work is to reduce the area of an adder and to reduce the delay due to carry propagation. We use the 24-transistor mirror FA as a base for our design, which is illustrated in Fig 5. To optimize the speed, two FAs are joined in a single block and the carry look-ahead technique is used to shorten the carry path within the radix-4 FA block. The transistor schematic is shown in Fig. 7. The total transistor count is 56. Boolean equations for the two carry and two sum gates of the carry look ahead design are given below.

$$\overline{C_1} = \overline{(A_0 + B_0)C_{in} + A_0.B_0}$$

$$S_0 = \overline{C_1}.B_0 + \overline{C_1}.C_{in} + \overline{C_1}.A_0 + A_0.B_0.C_{in}$$

$$C_{out} = (A_0 + B_0)(A_1 + B_1)C_{in} + A_0.B_0(A_1 + B_1) + A_1.B_1$$

$$S_1 = \overline{C_{out}.\overline{B_1} + C_{out}.\overline{C_1} + C_{out}.\overline{A_1} + \overline{A_1}.\overline{B_1}.\overline{C_1}}$$

The circuit for computing the least significant sum bit S0 is similar to radix-2 FA. But for most significant carry bit Cout, the carry look ahead technique is designed. Equation mentioned above is similar to the equation for a CLA with the difference that generate and propagate signals are computed explicitly for the CLA. To implement the function that computes the most significant sum bit S1 with a single gate, we invert the inputs A1, B1 and C1.

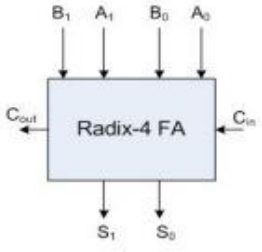

Fig. 6: Radix-4 FA block.

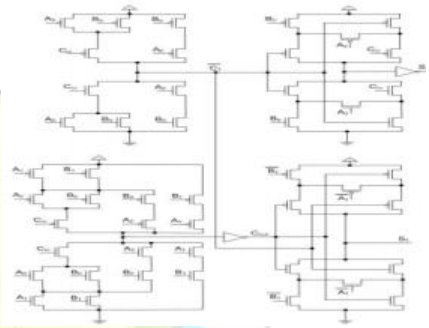

Fig 7: Radix-4 FA.

VI. SIMULATION AND COMPARISON

The tool used for simulation purpose is Tanner tool version 13.0. The design cycle for the development of electronic circuits includes an important Pre-fabrication verification phase.

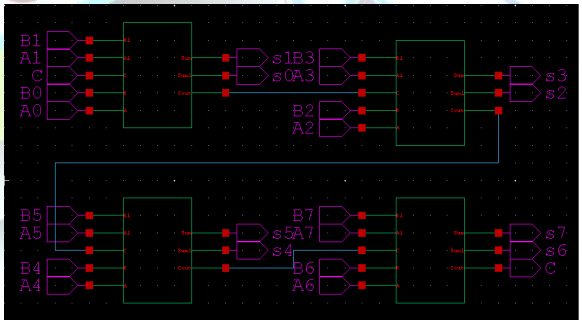

Fig 8: Radix-4 8 bit adder

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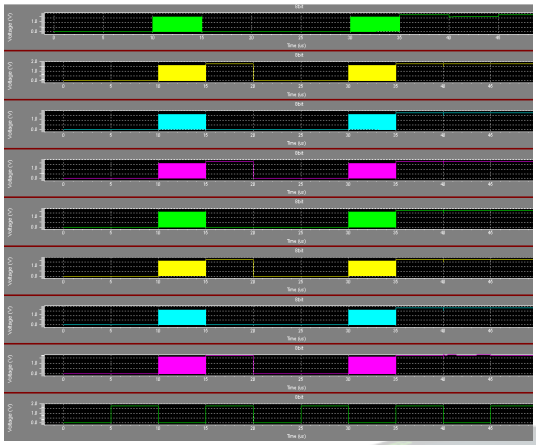

Fig 9: Recursive 8 bit adder Simulation result

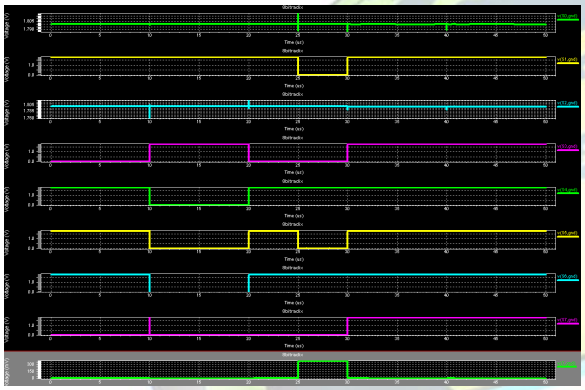

Fig 10: Radix-4 FA Simulation result

Parameter	8 bit Recursive Adder	8 bit Radix adder
Average Power (mW)	2.299	0.1195
Maximum Power (mW)	18.619 at time 2 * 10^{-5}	7.0817 at time 2 * 10^{-5}
Minimum Power (µW)	0.13906 at time 1 * 10^{-5}	0.0927 at time 1.000 * 10^{-5}

Fig 11: Comparison Table

As observed from the table about the two different adders that various designs have their own advantage and disadvantage in terms of area, delay and power consumption. So reducing any of these parameters will leads to a high performance design of full adder design. Hence we can see that radix 4 FA is better than recursive adder designs in terms of Power consumption, Number of Transistor, Delay, Power Delay Product. Future work will be focused on the reduction of any of the parameter shown above i.e. Area, Delay and Power. There is also another term called power delay product, this is generally used for to make a trade-off between power consumption and delay.

VII CONCLUSION

This brief presents an efficient implementation of a Modified PASTA. Initially, the theoretical foundation for a single-rail wave pipelined adder is established. Subsequently, the architectural design and CMOS implementations are presented. The design is compared with the Radix Approach which achieves a very simple n-bit adder that is area, power consumption wise much more efficient than the previous self timed adder. Moreover, the circuit works in a parallel manner for independent carry chains, and thus achieves logarithmic average time performance over random input values. The completion detection unit for the proposed adder is also practical and efficient. Simulation results are used to verify the advantages of the modified self timed adder.

REFERENCES

[1] Mohammed Ziaur Rahman, Lindsay Kleeman, and Mohammad Ashfak Habib, "Recursive Approach to the Design of a Parallel Self-Timed Adder," IEEE Transaction on Very Large Scale Integration (VLSI) Systems, vol. 23, no. 1, January 2015.

[2] M. Z. Rahman and L. Kleeman, "A delay matched approach for the design of asynchronous sequential circuits," Dept. Comput. Syst. Technol., Univ. Malaya, Kuala Lumpur, Malaysia, Tech. Rep. 05042013, 2013.

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Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
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[3] Christo Ananth, H. Anusuya Baby, "S-Box using AES Technique", International Journal of Engineering Research & Technology (IJERT), Vol. 3 Issue 3, March – 2014, pp 285-290

[4] D. Geer, "Is it time for clockless chips? [Asynchronous processorchips]," IEEE Comput., vol. 38, no. 3, pp. 18–19, Mar. 2005.

[5] A.J. Martin and M. Nystrom, "Asynchronous techniques for system-on-chip design," Proc. of the IEEE, vol. 94, no. 6, pp. 1089-1120, June 2006.

[6] F.-C. Cheng, S. H. Unger, and M. Theobald, "Selftimed carry-lookaheadadders," IEEE Trans. Comput., vol. 49, no. 7, pp. 659–672, Jul. 2000.

[7] D. Johnson and V. Akella, "Design and Analysis of Asynchronous Adders," IEE Proc. on Com. & Dig. Tech., vl4!i, nl, pp. 1-8, 1998.

[8] G.A. Ruiz and M.A. Monzano, "Compact 32-bit CMOS Adder in Multiple-output DCVS Logic for Self-timed Circuits," IEE Proc. Cir., Dev. &Sys., v147, n3, pp. 183-188,2000.

[9] J. Sparso and S. Furber, Principles of Asynchronous Circuit Design: A Systems Perspective: Kluwer Academic Publishers, 2001.

[10] M. Anis, S. Member, M. Allam, and M. Elmasry, "Impact of technology scaling on CMOS logic styles," IEEE Trans. Circuits Syst., Analog Digital Signal Process., vol. 49, no. 8, pp. 577–588, Aug. 2002.