ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 3, Special Issue 15, March 2016

RADIX 4 DUAL MODE SINGLE BINARYAND DOUBLE BINARY MLMAP DECODER FOR LOW POWER APPLICATIONS

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ABSTRACT

A Turbo decoder is typically one of the most computation-intensive parts in wireless receiver. Increased complexity and performance requirements and the need to reduce power and area are significant challenges for Turbo decoder hardware implementation. The iterative nature of turbo-decoding algorithms increases their complexity compare to conventional FEC decoding algorithms. Two iterative decoding algorithms, Soft-Output-Viterbi Algorithm (SOVA) and Maximum A posteriori Probability (MAP) Algorithm require complex decoding operations over several iteration cycles. So, for real-time implementation of turbo codes, reducing the decoder complexity while preserving biterror-rate (BER) performance is an important design consideration. The MAP algorithm is an optimal but computationally complex SISO algorithm. The Log-MAP and Max-Log-MAP algorithms are simplified versions of the MAP algorithm. So the Max-Log-MAP algorithm was proposed later to reduce the arithmetic complexity while still maintaining good decoding performance. The single bit or double bit can be decoded by dual mode radix 4 single binary (SB)/double binary (DB) algorithm also proposed in this paper. The Xilinx software used to execute the program.

Key words: SOVA, MLMAP decoder, radix 4 SB/DB decoding.

I.INTRODUCTION

Convolution coding is used in communication such as satellite and space communication to improve communication efficiency. The convolution code has enriched with the gift of a linear code with quality properties that it can operate on serial data as well as block codes. The convolution encoder with turbo decoder is a forward error correction method is mostly suited to a channel in which the transmitted signal is corrupted because of additive white Gaussian noise. IS-95, a wireless cellular standard for CDMA (Code Division Multiple Access), employs convolution coding which is the part of convolution coding .Convolutional encoding is a method of adding redundancy to a data stream in a controlled manner to give the destination the ability to correct bit errors without asking the source to retransmit. Convolutional codes, and other codes which can correct bit errors at the receiver, are called forward error correcting (FEC).

The decoding algorithm employed in the Turbo decoders is the maximum a posteriori (MAP) algorithm proposed and is also called the BCJR algorithm. The high complexity and long latency of the original MAP algorithm has made high-speed VLSI implementations extremely difficult to realize. Fortunately, many simplifications have been applied to the original MAP algorithm in order to reduce the implementation complexity.

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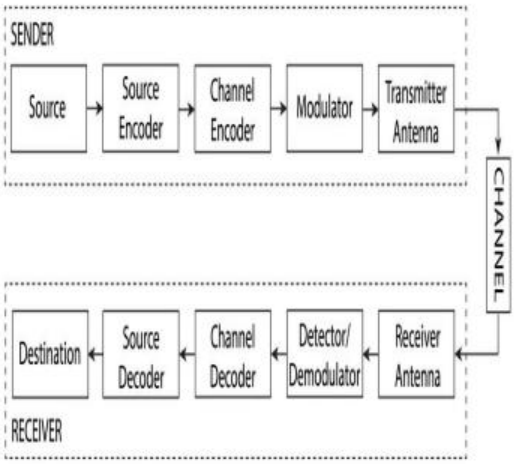

Fig.1 Digital Communication System

The decoding is based on the MAP algorithm and is usually calculated in the log domain to avoid multiplications and divisions. Christo Ananth et al. [10] proposed a system, Low Voltage Differential Signaling (LVDS) is a way to communicate data using a very low voltage swing (about 350mV) differentially over two PCB traces. It deals about the analysis and design of a low power, low noise and high speed comparator for a high performance Low Voltage Differential Signaling (LVDS) Receiver. The circuit of a Conventional Double Tail Latch Type Comparator is modified for the purpose of low-power and low noise operation even in small supply voltages. The circuit is simulated with 2V DC supply voltage, 350mV 500MHz sinusoidal input and 1GHz clock frequency. LVDS Receiver using comparator as its second stage is designed and simulated in Cadence Virtuoso Analog Design Environment using GPDK 180nm .By this design, the power dissipation, delay and noise can be reduced.

III.TURBO DECODER

Turbo decoding is based on the principle of comparing the probability of a received soft input data being a '1' and '0'. The Turbo Decoder uses a decoding scheme called the MAP (Maximum A posteriori Probability) algorithm. The algorithm determines the probability of whether each received data symbol is a '1' as well as a '0'. This is done with the help of the data, parity symbols, and the decoder knowledge of the encoder trellis. A trellis is a form of a state transition table, of the encoder input/output]. Based on the data and parity information, the MAP decoder computes the probability of the encoder being in a particular state.

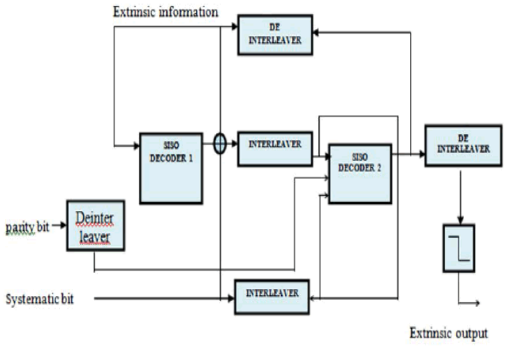

Fig.2 Iterative turbo decoder

The computation of the probabilities is done iteratively to obtain a reliable result. Once the result is considered reliable, one can make a final decision as to whether the data symbol is a "1" or "0".

$$L(D)=\log\frac{P(D=0)}{P(D=1)}$$

The Log Likelihood Ratio is the probability that the received data bit is a „0" divided by the probability that the received data bit is a '1'. Thus, taking the logarithm we will have a positive value if P(D=1) > P(D=0), and negative value for the opposite. A positive value means the data value is a "1", otherwise a "0". For one complete cycle of iteration, one needs to compute the LLR using parity for non-interleaved as well as interleaved data.

IV.OVERVIEW OF TRELLIS DIAGRAM

A.RADIX 2 TRELLIS DIAGRAM

Figure 3 shows the trellis diagram of a rate1/2 code with constraint length K = 2. The states are depicted as nodes, which denote the memory contents of the convolutional encoder.

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Each state has two branches, each of which corresponds to one of two possible input values.

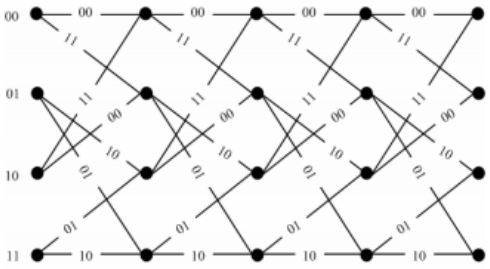

Fig.3 Rate ½ code radix 2 trellis diagram

The branches of the trellis diagram are labeled with two bit branch words corresponding to the associated state transitions.

B.RADIX 4 TRELLIS DIAGRAM

The radix-4 butterfly is applied to the MAP decoder design to increase the decoding speed of the turbo decoder. Figure 4 shows the radix-4 trellis corresponding to the radix-2 trellis in Fig. 3. Two stage radix-2 trellis can be merged to one stage radix-4 trellis by rearranging the states appropriately.

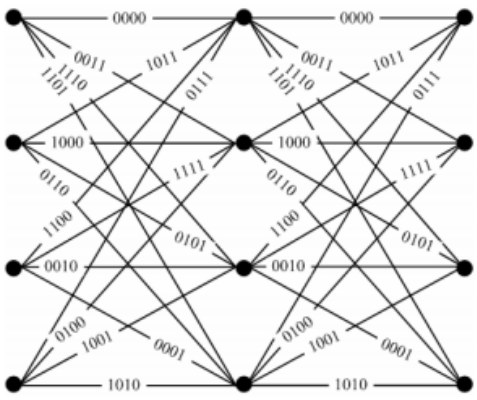

Fig.4 The radix-4 trellis diagram

Notably, each branch of a radix-4 butterfly has 4-bit branch words, and corresponds to two input bits. Merging the trellis does not affect the selection of the most-likely bit, since a one-to-one mapping exists between the shortest path in the radix-4 trellis and the original radix-2 trellis. Each radix-4 butterfly in the radix-4 trellis has four origin and destination states, and 16 branches.

Figure 5 shows a radix-4 butterfly and its corresponding two stage radix-2 butterfly. Each branch of a radix-4 butterfly is a combination of two branches. For example, the branch word b_{00x00} in the radix-4 butterfly is combined from the branch words b_{00x0} at the first stage and b_{0x00} at the second stage, as shown in Fig. 5, and is given by $b_{00x00} = b_{00x0b0x00}$. Similarly, the branch b_{10x01} in the radix-4 butterfly is combined from the branch b_{10x0} at the first stage and b_{0x01} at the second stage, and is given by $b_{10x01} = b_{10x0b0x01}$.

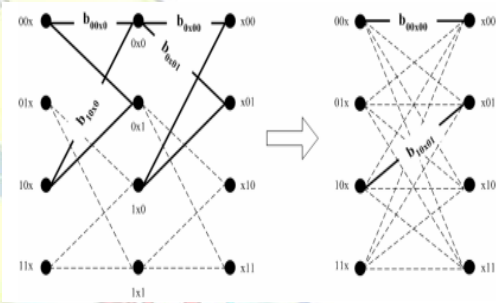

Fig.5 Radix 2 to radix 4 trellis conversion

According to the symmetry, only the eight branch metrics need to be computed, and the other eight branch metrics, can be derived from the computed branches.

V.MAP DECODER

Turbo decoders require soft-input soft-output decoding algorithms, among which the maximum a posterior probability (MAP) algorithm is widely adopted for its excellent performance for high throughput; highly parallelized decoder architectures are needed. Turbo-Decoders consist of component decoders which exchange information iteratively. Between iterations, this information is reordered following an interleaving scheme. MAP decoders are superior with respect to communications performance and for that reason preferred in advanced implementations.

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VI.MLMAP DECODER

The ML-MAP algorithm can be used for reduced complexity decoder implementation .The decoding process in MAP algorithm performs calculations of the forward and backward state metric values to obtain the log likelihood ratio (LLR) values, which have the decoded bit information and reliability values. The input sequence consisting of information bits X_k parity bits Y_k may include additive white Gaussian noise at time k. The MAP decoded output, the log-likelihood ratio of information bits d_k can be derived from Equations.

The log likelihood ratio values are calculated by the following equation:

$$L(d_m) = ln\frac{\sum_{S_m}\sum_{S_{m-1}}\gamma_1(S_{m-1},S_m)\alpha(S_{m-1})\beta(S_m)}{\sum_{S_m}\sum_{S_{m-1}}\gamma_0(S_{m-1},S_m)\alpha(S_{m-1})\beta(S_m)}$$

Forward state metric can be calculated by

$$\alpha(S_m) = ln\sum_{S_{m-1}}\exp\left(\ln\gamma\left(S_{m-1},S_m\right) + \ln\alpha(S_{m-1})\right)$$

Backward state metric can be calculated by

$$\beta(S_m) = ln\sum_{S_{m+1}}\exp\left(\ln\gamma\left(S_m,S_{m+1}\right) + \ln\beta(S_{m+1})\right)$$

where the branch metric (γ) is calculated by the a priori information (Le), channel reliability value (Lc), input symbols (x and y1), the systematic bit (ums) and the paritybit (ump).

The above equations consists logarithm function. So, it is converted into max log function by the well know approximation, called Jacobi algorithm and which is given below,

$\ln(e^x+e^y)=\max(x,y)+\ln(1+e^{-|x-y|})$

VI.DUAL MODE MLMAP DECODING

To support the multistandard CTC schemes, we intend to design dual-mode computational modules of the alternative SB and DB MAP decoding with high hardware usages andfully-shared storages. For the dual-mode MAP decoding, it is straightforward to implement the radix-4 SB and DB MAP decoding because of their similar radix-4 trellis structure. The dual-mode branch metrics decomposition is proposed to substitute the conventional BMU for the first and second stages of the BMU (BMU-S1 and BMU-S2) and to reduce the size of the BMC.

A.BRANCH METRICS DECOMPOSITION FOR RADIX-4 SB/DB MAP DECODING

For the both radix-4 SB and DB MAP decoding, the BMU and BMC designs become critical because 16 branch metrics are generated and stored. The decomposed branch metrics ofthe radix-2 SB MAP decoding was proposed to reduce the storages of four branch metrics. Partial data of the branch metrics generated by the BMU-S1 are stored into the BMC which is smaller than the conventional one. When the real branch metrics are required, they are calculated by the BMU-S2with the stored partial data. In addition, the stored partial data are also used to generate the extrinsic information. The partial data of branch metrics of the radix-4 SB MAP decoding are defined as,

$$\Gamma^0_{s,k} = -\Lambda_{apr,k-1}(u_{k-1}) - \Lambda_{apr,k}(u_k) - y^s_{k-1} - y^s_k$$
$$\Gamma^1_{s,k} = -\Lambda_{apr,k-1}(u_{k-1}) + \Lambda_{apr,k}(u_k) - y^s_{k-1} + y^s_k$$
$$\Gamma^2_{s,k} = \Lambda_{apr,k-1}(u_{k-1}) - \Lambda_{apr,k}(u_k) + y^s_{k-1} - y^s_k,$$
$$\Gamma^3_{s,k} = \Lambda_{apr,k-1}(u_{k-1}) + \Lambda_{apr,k}(u_k) + y^s_{k-1} + y^s_k$$
$$\Theta^0_{s,k} = y^p_{k-1} + y^p_k$$
$$\Theta^1_{s,k} = y^p_{k-1} - y^p_k.$$

The BMC only stores the above value instead of the 16 branch metrics.

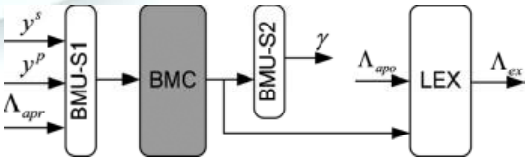

Fig.6 Block diagram of the branch metrics decomposition.

The partial data of branch metrics of the DB MAP decoding are defined as

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$$\Gamma^0_{d,k} = \Lambda^{(00)}_{apr,k}(u_k) - 2y^{s1}_k - 2y^{s2}_k$$
$$\Gamma^1_{d,k} = \Lambda^{(01)}_{apr,k}(u_k) - 2y^{s1}_k + 2y^{s2}_k$$
$$\Gamma^2_{d,k} = \Lambda^{(10)}_{apr,k}(u_k) + 2y^{s1}_k - 2y^{s2}_k$$
$$\Gamma^3_{d,k} = \Lambda^{(11)}_{apr,k}(u_k) + 2y^{s1}_k + 2y^{s2}_k$$
$$\Theta^0_{d,k} = 2y^{p1}_k + 2y^{p2}_k$$
$$\Theta^1_{d,k} = 2y^{p1}_k - 2y^{p2}_k.$$

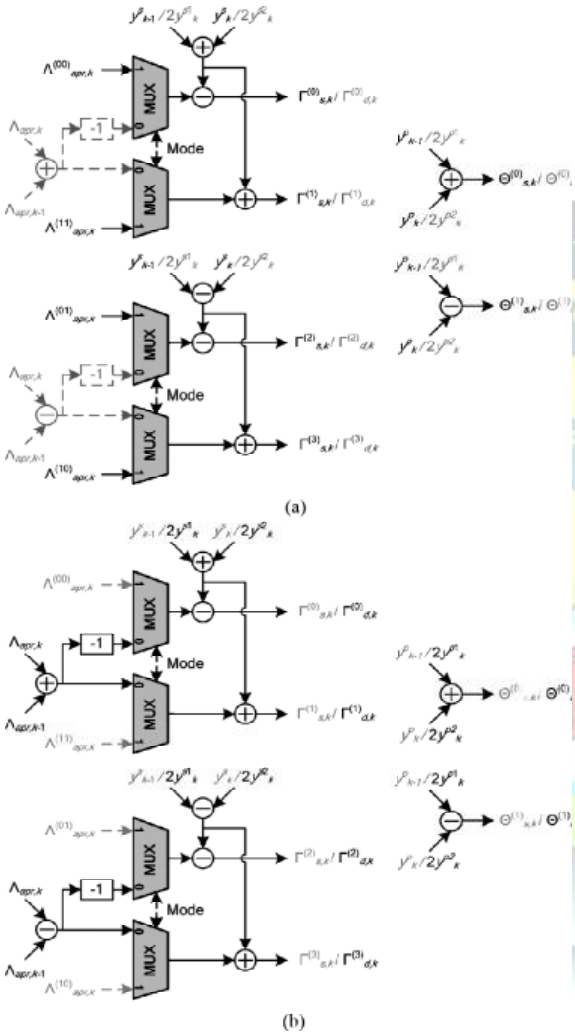

Fig.7 Dual-mode first stage of the BMU (BMU-S1) of the branch metrics decomposition: active logic blocks (a) in SB mode and (b) in DB mode.

The BMC only stores the above values instead of the 16 branch metrics.

1. RADIX-4 SB MAP DECODING

The SB CTC encodes one binary bit u_k at time k. For decoding two binary bits at a time, the radix-4 SB ML-MAP algorithm has been derived in by a look-ahead technique. The arithmeticoperations of the radix-4 SB ML-MAP are described as follows.

$$\alpha_k(S_k) = \max_{S_{k-1},S_{k-2}} (\gamma_k(S_{k-2},S_k) + \alpha_{k-2}(S_{k-2}))$$

$$\beta_k(S_k) = \max_{S_{k+1},S_{k+2}} (\gamma_{k+1}(S_k,S_{k+2}) + \beta_{k-2}(S_{k-2}))$$

$$\gamma_k(S_{k-2},S_k) = \Lambda_{apr,k-1}(u_{k-1}) + y_{s(k-1)}x_{s(k-1)} + \sum_{i=1}^{m} y^{pi}_{k-1}\, x^{pi}_{k-1} + (\Lambda_{apr,}k(u_k) + y_{sk})x_{sk} + \sum_{i=1}^{m} y_{pk}\, x_{pk}$$

2. RADIX-4 DB MAP DECODING

In DB mode two binary bits are encoded u_k=$u1_k$,$u2_k$. The arithmetic operations of the of the Radix-4 DB MAP are described as,

$$\alpha_k(S_k) = MAX_{S_{k-1}}(\gamma_k(S_{k-1},S_k) + \alpha_{k-1}(S_{k-1}))$$

$$\beta_k(S_k) = MAX_{S_{k+1}}(\gamma_{k+1}(S_k,S_{k+1}) + \beta_{k+1}(S_{k+1}))$$

$$\gamma_k(S_{k-1},S_k) = \Lambda^{(z)}_{apr,k}(u_k = z) + 2y^{s1}_k x^{s1}_k + 2y^{s2}_k x^{s2}_k + 2\sum_{i=1}^{m} y^{pi}_k\, x^{pi}_k$$

VII.DUAL MODE LLR CALCULATION

The high hardware usage of the dual-mode LAPO, a-posteriori LLR can be achieved by rewriting the operations by using MAX operation. The "Mode" is used to select the mode of operation (SB or DB). When "Mode" is active low, the dual-mode LLR calculator is in SB mode. When "Mode" is active high, the dual-mode LLR calculator is in DB mode. In the dual mode architecture, some of the connections are dummy.

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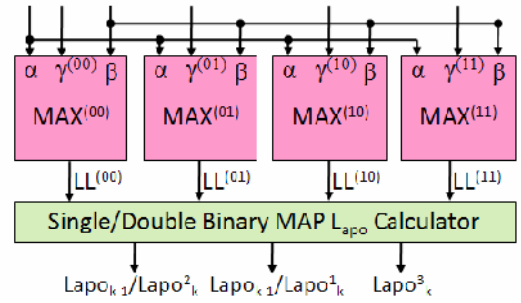

Fig.8 The LLR calculation block diagram of the dual-mode ML MAP Decoder

VIII.RESULTS AND DISCUSSION

In this paper first analyze the radix 2 trellis and then construct the radix 4 trellis by combining the two stages in the radix 2 trellis. The present research is focused on the design and development of dual mode SB/DB MLMAP decoder for low power applications. Next analyze the performance of the MLMAP decoder using various parameters for low power design.

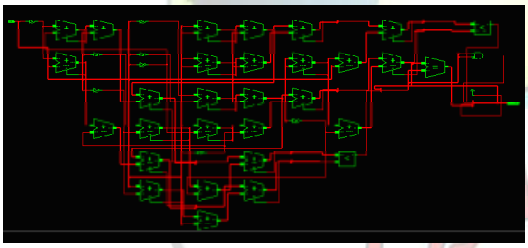

Fig.9 RTL schematic view

Table 1.Comparison of power consumption of MLMAP Decoder

FPGA Family	Device Specifications	Power Consumption
Spartan 3E	Xc3s1200E	155.9mW
Spartan 3E	Xc3s500E	155.9mW
Spartan 3E	Xc3s250E	52.58mW

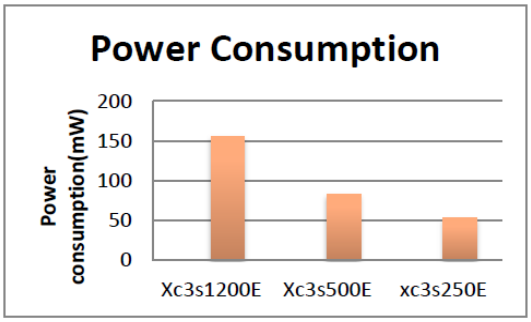

Fig .10. Power Consumption Chart

IX.CONCLUSION

In this paper, principles of turbo decoding and its applications in wireless communications have been discussed. The concept has been given to modify the equation on an algorithm to improve the BER performance of the Max-Log-MAP algorithm which is the reduced complexity version of the Log-MAP algorithm. The performance gap between the Max-Log-MAP and Log-MAP algorithms can be overcomes by reduced computational complexity. The hardware shared dual mode MAP decoder achieves low computational cost and low memory storages. This MLMAP processor achieves high throughput rates and high area efficiency.

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