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DESIGN OF WALLACE TREE MULTIPLIERUSINGHYBRID ADDER

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ABSTRACT: Adders are the most important building block in a wide variety low power VLSI system design [2]. These adders are mainly used in other basic digital operations such as subtraction, multiplication and division. Here hybrid adder is used as full adder to design a 4*4 Wallace tree multiplier. The design of hybrid adder for low power is obtained and the low power units are implemented on the proposed design of multiplier and the results are analyzed for obtaining better performance. Lowering the number of transistors can naturally lead to smaller occupied area, higher speed and lower power consumption. There are 12 transistors needed to design a hybrid adder reported to have better performance than others, are reviewed and analyzed. The performance analysis of Wallace tree design using basic full adder, conventional CMOS full adder and proposed hybrid full adder are to be executed and analyzed. From the analysis low power and area efficient Wallace tree multiplier was designed in TANNER v14.1.

Keywords- Full adder, Hybrid adder, CMOS, Wallace tree multiplier

I INTRODUCTION

Multiplier is one of the key hardware blocks in many systems. With growing technology, many researchers have taken much effort to design multipliers which offer the important considerations such as high speed, low power consumption, thus making them compatible for various high speed, low power, and compact VLSI implementation. Area, speed and power are conflicting constraints [8]. Therefore we try to improve speed, area and power is also affected. Multipliers in digital circuit design are often divided into two subgroups: Array and tree multipliers. Array multipliers use a rigid pattern to construct their multipliers and multiplication process involves multiplication of partial product and higher order addition. This leads to compact designs and an commonly distributed delay. Tree multipliers on the other hand to reduce the number of bits in each level in the tree until the calculation is done. Since this produces a complex tree structure, the delay is not commonly distributed. [5] This may create glitches that use power, and the tree structure uses a lot of interconnection, end therefore uses a lot more area. The depth of an array multiplier is $O(n) = n$ while it is $O(n) = \log 2n$ for multiplier trees Even though the wiring cause more delay for multiplier trees, it still perform faster than array multipliers.In array multipliers, the counters and compressors are connected in a serial system design for all bit slices of the Partial Product parallelogram.

The terms are summed by an array of n [n – 2] full adders and n half adders.A multiplier essentially consists of two operands, a multiplicand "A" and a multiplier "B" and produces a product term "P". In the initial stage, the multiplicand and the multiplier are multiplied bit by bit to generate the partial product terms. In second stage, it is the most difficult and determines the overall speed of the multiplier. This stage includes addition of these partial product terms to generate the product term "P". This work will be more focused on the optimization of this stage, which consists of the addition of all the biased products. If speed is not an issue, the partial products can be added in order, reducing the design complexity. The shifting of partial products for their proper alignment is performed by simple routing and does not require any logic. The number of rows in array multiplier denotes length of the multiplier and width of each row denotes width of multiplicand. The output of each row of adders acts as input to the next row of adders.Wallace trees are irregular structure in that the informal explanation does not specify an efficient method for the compressor interconnections. But it is an efficient method of adding partial products in parallel [4].The Wallace tree multiplier architecture comprises of Adders for computing and adding the partial products so obtained and a carry propagate adder is in the final stage of addition.Given 4*4Wallace multiplier has 12 full adders, where all these full adders are replaced by proposed hybrid full adders. By using these basic adders dynamic power dissipation in the multiplier is reduced such that half of the total leakage power in the 4*4 Wallace tree multiplier is reduced [1]. A basic multiplier consists of three parts (i) partial product generation (ii) partial product addition and (iii) final addition. Here the hybrid adder is designed using 22 transistors and 12 transistors in S-Edit v14.11. From the analysis hybrid full adder is designed and replaced as full adder and result is estimated using TANNER 0.18 µm CMOS technologyand waveform simulated.

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IISTUDY OF VARIOUS MULTIPLIERS

Carry-Save Multiplier

Carry Save Array Multipliers have a regular structure,which makes it acquiescent to mechanization.The algorithmis based on the fact that the multiplication resultdoes not change when the output carry bits are passeddiagonally downwards instead of using only to the right. This is called the carry-save multiplier becausethe carry bits are not immediately added but are rathersaved for the next step of addition stage [4].In the final stage of CSA thecarries and the sums are combined in a fast-carry propagateadder stage by using a carry-lookahead adder.Due to the additional adder in each stage there is a smallincrease in the area cost. It can also be easilypipelined.Another added advantage is that there is onlyone critical path rather than the number of identical criticalpaths found in the generic array multiplier.The generalstructure of a Carry-Save Multiplier is shown in Fig.1**.** The delay of this multiplier can be expressed as,

$$\Delta T = T\text{and} + T\text{final} + X - 1T\text{carry}$$

Where*T*and is the delay of the product generating ANDgates, *T*final is the delay of the final stage carry-lookaheadadder, *X* is the number of partial product stages, and *T*carry is the propagation delay between input and output carry.

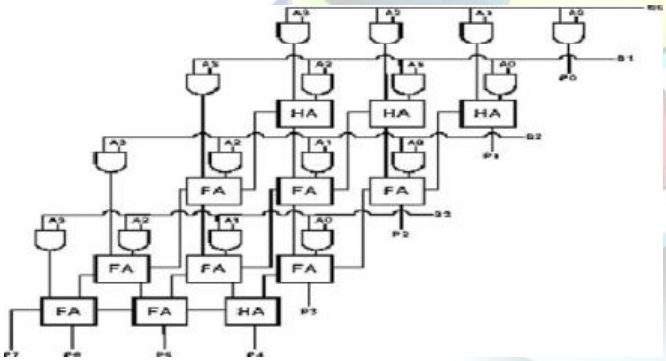

Fig.1 Carry SaveArray Multiplier

Bit Array Multipliers are very regular structuresand are simple to expand.The structure is similar to the Carry-Save multiplier but propagatesthe carry bits from the full adders in a different manner.A simple diagram of a 4×4 CSA multiplier is shown in Fig.1. Each partial product is generated by the multiplicationof the multiplicand with one multiplier bit.Thepartial products are shifted according to their bit ordersand then added.In array multiplication we need to addas several partial products as there are multiplier bits.Inorder to perform signed multiplication with efficient method has 2's complement number system is used to represent the multiplicand and the multiplier.To achieve this operation, thesign bits of the partial products in the initial row and thesum and carry signals of each adder stage are extended.The extension is carried out until the signal width matchesthe width of the largest absolute value signal in that stage.The array structureis a difficult task to measure the propagationdelay.

$$\Delta T = T\text{and} + T\text{sum} + Y - 1 + X - 2T\text{carry} \quad (4)$$

where *T*and is the time delay of the pre-product generating ANDgates, *T*sum is the time delay between the input carry and the sumbit of the full adder, *Y* is the width of the multiplicand, *X*is the width of the multiplier, and *T*carry is the propagationdelay between input and output carry.

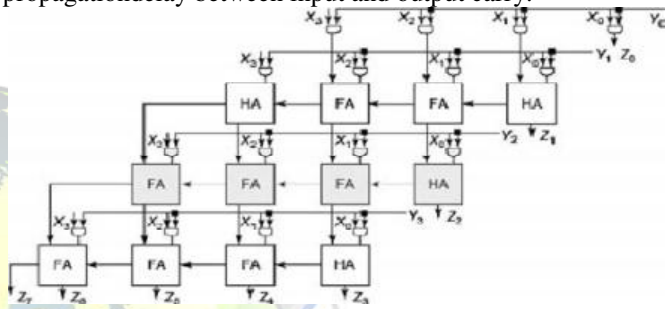

Fig.2 Bit Array Multiplier

Wallace trees were first introduced in order todesign the multipliers whose completion time grows as thelogarithm of the number of bits to be multiplied should be increased.Wallace tree multiplier is based on tree structure [1][4].In Fig.3, 4 bit Wallace tree multiplier is shown. Wallacemethod uses three-steps to process the multiplicationoperation

(i). Formation of bit products
(ii).The bit product matrix is reduced to a 2-row matrixby using a carry-save adder (Wallace tree).

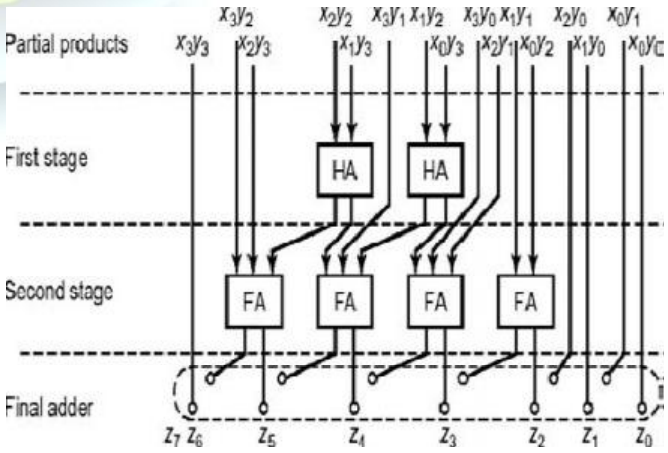

Fig.3 Multiplication Function of Wallace Tree multiplier

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The work has been taken in this project is based on design the Wallace tree multiplier structure shown below [8]

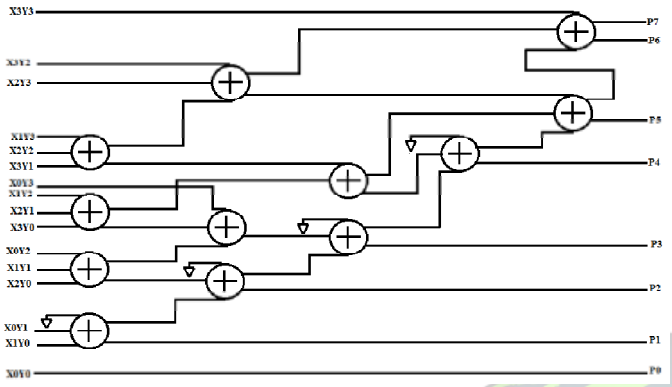

Fig.4 Structure of Wallace Tree Multiplier

Number of full adders varied according to the structure of wallace tree multiplier. For an existing design, wallace tree multiplier was designed with 12 full adders and a multiplexer. The above design shows multiplier designed by using 12 full adders. If the design was done by using both half adders and full adders, which leads to increased area. Compared to other multipliers, wallace tree multiplier leads to reduced area and power consumption.

InConventional CMOS Full Adder cell, which contains the 22 transistors, a modified low-power XOR/XNOR circuit. In this circuit worst case delay problems of transitions from 01 to 00 and from 10 to 11 are solved by adding two series PMOS and two series NMOS transistors respectively. The adders considered in this work were designed using traditional implementing methods, i.e. [8]they use only transistors and no input capacitors are used.

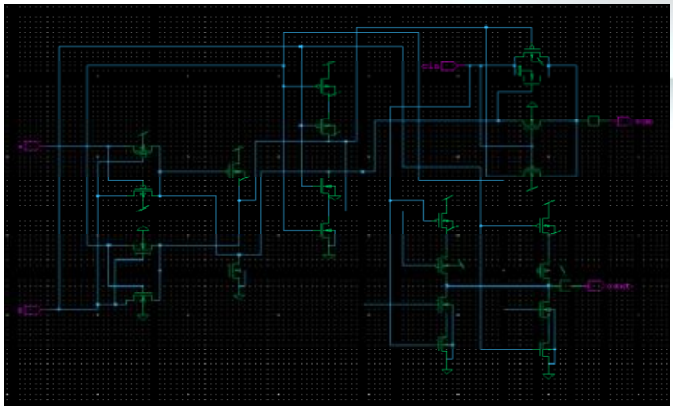

Fig.5 Existing Conventional CMOS Full Adder Design

III ANEW IMPLEMENTATION OF WALLACE TREE MULTIPLIER

a. Proposed Design Of Hybrid Full Adder

In an existing system the hybrid full adder is designed by using 22 transistors. From the design, number of parameters such as transient time, area and power consumption were analyzed. In proposed design the same hybrid full adder is designed using 12 transistors, it shows reduced power consumption and area. From the analysis the wallace tree multiplier is designed using this proposed hybrid full adder.The transistor connection for acomplementary switch or transmission gate which consistsof an n-mos and p-mos transistor connected inparallel with separate gate connection. The controlsignal is applied to the gate of n-mos, and itscomplement is functional to the gate of the p-mos device. Nmospass transistor is good for transmission of '1'and poor for transmission of '0'.p-mos passtransistor is good for transmission of '0' and reducedfor transmission Of '1'. The circuit of the 12 passtransistor adder is shown in Fig.5.This result shows better performance regarding speedand low power consumption [6]. The output voltageswing will be equal to the VDD, if a driver is used atthe output of design.

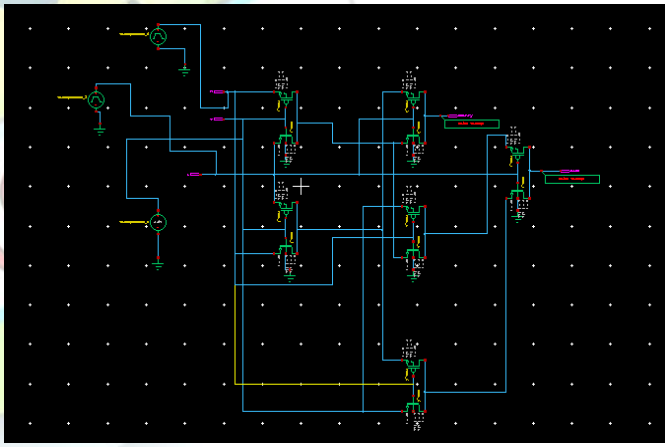

Fig.6 Proposed Hybrid full adder

b. Proposed Design Of Wallace Tree Multiplier

The basic design of Wallace tree multiplier using full adder having enlarged area [2]. Due to using gates for designing full adder leads to increased area and time required to execute the design will be increased. The average transient time analysis for the design of wallace tree multiplier using basic full adderhaving 0.59 seconds. Similarly the same wallace tree multiplier designed by using Conventional CMOS full adder having transient time analysis of 0.67 seconds. The reduced number of transistor count leads to reduced power consumption and area. These two factors are important considerations of low power VLSI design. Here the full adder

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is designed using 12 transistors i.e, Hybrid adder. Various multipliers were designed and analyzed for obtaining better performance such as the important phenomena of Area and Power consumption.

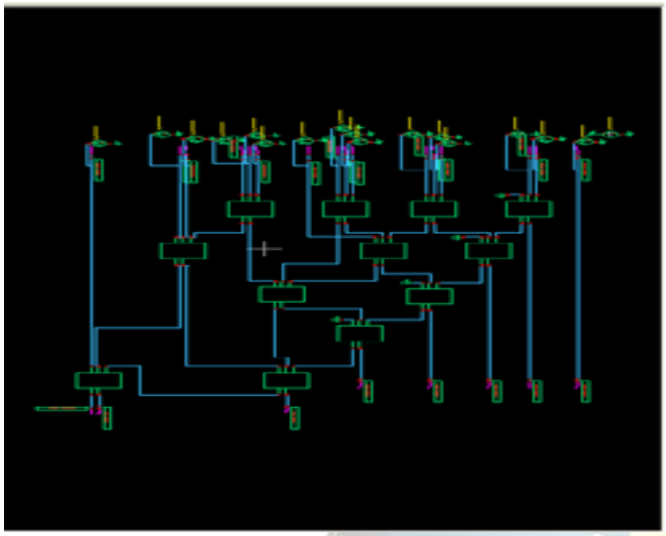

Fig.7 Proposed design of Wallace tree multiplier

Wallace Tree Multiplier	Transient Time(sec)	Power Consumption
Multiplier using Conventional CMOS Full adder	0.67	10.078mw
Multiplier using Full adder	0.52	3.9556mw
Multiplier using Proposed full adder	0.45	6.4944µw

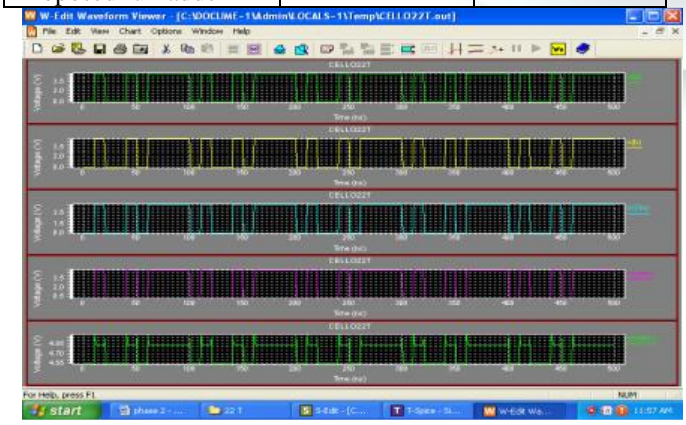

Fig.8 Waveform of Conventional CMOS Wallace tree multiplier

The comparison between various multipliers depends on the design with number of transistors and its design area.

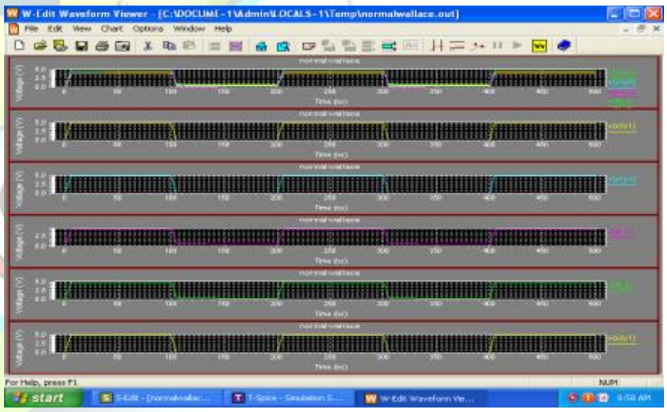

Fig.9 Waveform of Wallace tree multiplier

Table 1. Comparison of Various Multipliers

IV CONCLUSION

The power performance characteristics of Wallace tree multiplier using Conventional CMOS full adder and proposed hybrid 12 transistor fulladders were performed and analyzed. The main objective of VLSI design is to reduce the power consumption and area,here the proposed method of designing the hybrid adder exhibits better powerperformance than the existing 22 transistors Conventional CMOS Full adder design. Due to the reduction of area and power consumption in this proposed system will automatically reduce the transient time

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of Wallace tree multiplier over the existing designs. In future, Array multiplier can be designed by using the same Hybrid Full adder design.

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