Design of Synchronous cyclic code counter used by novel Reversible Gate

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***Abstract*——** **This paper presents a new reversible gate for designing an Synchronous cyclic code counter.Reversible logic has considered now a days in quantum computing,modern nano technology& optical computing due to its higher performance,low power dissipation. This paper presents various classical operations of the proposed reversible gate. The proposed reversible gate is better for designing reversible counter compared to those gates required in the other literature. These Synchronous counter gives the initial threshold for more complex structures. Since the output of the sequential circuit depends not only on the present inputs but also on the past outputs,so the construction of the sequential circuit is more complex than that of combinational circuit. This paper has been developed as part of low power processor design in the platform Xilinx ISE 9.2 and synthesized on 90nm Spartan-3E FPGA.**

***Index Terms*—Quantum computing,optical computing,DNA Computing, Reversible logic,Flip flop,Synchronous counter.**

INTRODUCTION

A reversible logic gate is an n-input n-output logic device with one-to-one mapping. This helps to determine the outputs from the inputs and also the inputs can be uniquely recovered from the outputs. Reversible computing may be defined as performing computing in such a way that earlier state of computation may be reconstructed from the future states.Many scientists had already discussed more about reversible logic. Some of them are as follows:[1] In 1961,Landaeur states that one bit loss in digital circuits produces a small amount of heat dissipation in the order of kTln2.[2] Benett showed that in order to avoid kTln2 of power dissipation,it must be built using reversible logic.[3] In 1965,Gordon E.Moore predicted that the number of components on the chip will increase every 18 months which is known as Moore's law.Later in 1980. Perkowski et.al.'s states [4] "every future technology will have to use reversible gates in order to reduce power" Thishas led many people to pursue research in the area of reversible logic.According to Frank [5] ...computers based mainly on reversible logic operations can reuse a fraction of the signal energy that theoretically can approach arbitrarily near to 100% as the quality of the hardware is improved. In [6] Toffoli states.... using invertible logic gates, it is ideally possible to build a sequential computer with zero internal power dissipation. Thomos Toffoli was the first person who proved that reversible counter been designed by sequential circuit.The effect of Moore's Law was studied carefully & researchers have made that the power dissipation will increase when the number of components on the chip increase.Hence power minimiztion has prfy6jo9l9ojm6y5dbecome a major issue for today designing area of VLSI

The main purpose of designing reversible losic is to reduce power dissipation,cost,complexity. In reversible circuits number of inputs & outputs must be equal.A reversible logic function is defined as a function for which each input vector maps in to a unique output vector.It is always possible to find out the inputs from outputs since there is a one to one relationship between the input & the output.A reversible logic circuit should have the following feautures: Using minimum number of reversible gates,reuces circuit complexity,cost & power dissipation.They donot allow fanouts.It must use a minimum depth or gate level.Sine the output of sequential circuit depends not only on the present inputs but also on the past outputs,so the design of sequential circuit is more complex than that of combinational circuit.

BASIC REVERSIBLE LOGIC GATES:
There are many reversible gates.They are
1.Peres Gate:

The input vector is I (A, B, C) and the output vector is O (P, Q, R). Peres gate is used because of its lowest quantum cost.

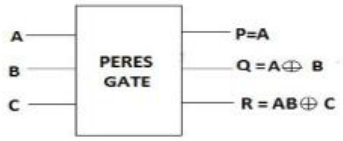

Fig 1: Peres Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

TRUTH TABLE FOR PERES GATE

2.Feymann Gate:

It is a 2*2 reversible gate. Its input vector is I(A,B) & output vector is O(P,Q).This gate can be used as a copying gate.Since fanout is not allowed in this gate,it can be used as duplication of outputs. Feynman gate is also known as CNOT (Controlled Not) gate.
The two key reasons to use this gate in reversible circuit are:

i) make the copy of an input (putting any of the input a constant 0)
ii) to invert an input bit (putting any of the input a constant 1) It is used to copy the input without producing garbage bits with B=0.

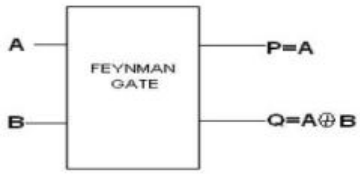

Fig 2: Feynman Gate

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

TRUTHTABLE FOR FEYMANN GATE

3. Toffoli Gate:Toffoli gate plays an important role in the reversible logicsynthesis. It is also used in the design of any Booleanfunction and hence it can be considered as a universalreversible gate.

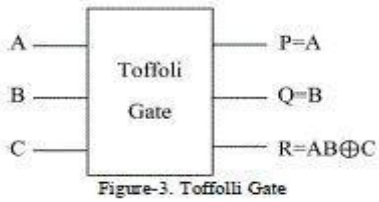

Figure-3. Toffolli Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

TRUTHTABLE FOR TOFFOLI GATE

4.Fredkin Gate:

The Fredkin gate is a reversible 3-bit gate that swaps the last two bits if the first bit is 1, i.e., a controlled-swap operation.Fredkin gate also has its importance in reversible literature as it is a 1-through gate (one input is directly generated as output) and two other outputs can generate two different Boolean functions. Fredkin gate is the mostly used reversible gate to design reversible latches. It can be used to implemant a Multiplexer.

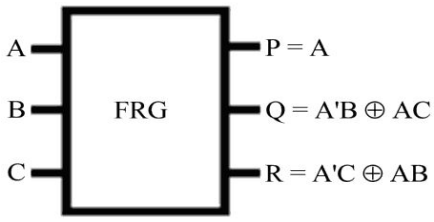

Figure_4 Fredkin Gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

TRUTHTABLE FOR FREDKIN GATE

RELATED WORKS ON REVERSIBLE COUNTER

Researchers have worked on many ways on sequential circuit and work is still going on. This section reviews some previous implementation and sequential circuit designs. Researchers [10, 12-15] proposed the implementation of all types of latches, flip-flops and their master-slave design. These works opens a door to the implementation of large sequential circuit like counter.

The authors [16-17] carry the above success to the of design reversible counter. Some of the works are implemented by the replacement of latches and gates by their reversible counter parts. Recently Khan [16] used Positive Polarity Reed Muller (PPRM) expression to design synchronous counter. All these works suggest that there is scope for the design and implementation of large sequential circuits like counter.

DESIGN AND SYNTHESIS OF REVERSIBLE COUNTER

This section describes our proposed design for n bit counter. Designs for both the asynchronous counter andthe synchronous counter are presented here. While designing counter, this paper also proposed the design of reversible T flip-flop which is the building block of the counter. This paper presents the design of T flip-flop, gated T flip-flop and master slave T flip flop. A T Flip-flop can be realized by a single Feynman gateThe following steps are required to design a sequential circuit.

1. Describe a general sequential circuit in terms of its basic parts andits input and outputs.
2. Develop a state diagram for a given sequence.
3. Develop a next-state table for a specific counter sequence.
4. Create a FF transition table.
5. Use K-map to derive the logic equations.
6. Implement a counter to produce a specified sequence of states.

CLK	T	Q_{N-1}	Q
0	0	0	0
1	0	0	0
0	0	1	1
1	0	1	1
0	1	0	0
1	1	0	1

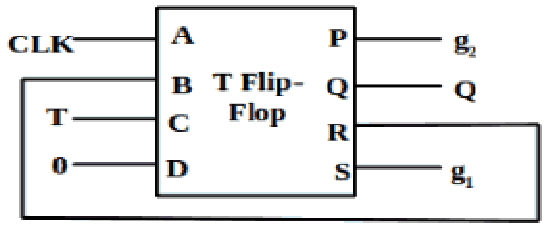

Figure_5 T Flip flop

INPUTS			OUTPUTS		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	1	1	0
0	1	0	1	1	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	1	0	1
1	1	0	0	0	1
1	1	1	0	1	0

IMPLEMENTATION OF 4 BIT ASYNCHRONOUS COUNTER

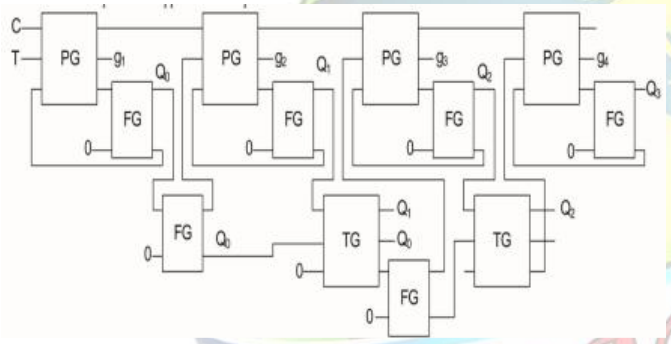

Figure_6: 4 BIT ASYNCHRONOUS COUNTER

Feymann,Toffoli & Peres gate are used to design a 4 bit synchronous counter.Synchronous counter is different from the asynchronous counter in that the clock pulses are given to inputs of all the flip flops at a time. Christo Ananth et al. [10] proposed a system which contributes the complex parallelism mechanism to protect the information by using Advanced Encryption Standard (AES) Technique. AES is an encryption algorithm which uses 128 bit as a data and generates a secured data. In Encryption, when cipher key is inserted, the plain text is converted into cipher text by using complex parallelism. Similarly, in decryption, the cipher text is converted into original one by removing a cipher key. The complex parallelism technique involves the process of Substitution Byte, Shift Row, Mix Column and Add Round Key. The above four techniques are used to involve the process of shuffling the message. The complex parallelism is highly secured and the information is not broken by any other intruder. It also improves power dissipation, consumes time & delay.

Theorem 1: To construct n bit asynchronous counter, if g is the total number of gates required to design the counter producing b number of garbage outputs then g≥2n and b≥n.
Proof: Each flip-flop consists of two gates; n bit counter requires n number of flip-flops. No additional gates are required to interconnect each other. So total number of gates required to design the counter is 2n, hence g≥2n. Similarly, every flip-flop produces only one garbage output. No garbage output produced while interconnection among flip-flops. So the total number of garbage out is n, hence b≥n.
Theorem 2: The quantum cost of an n bit asynchronous counter is Qn≥6n-1.
Proof: For n=1, only one Peres gate and one Feynman gate is required to construct the counter. The quantum cost of Peres gate is 4 and quantum cost of Feynman gate is 1. So the total cost 4+1=5.
Now for n>1, one Peres gate and one double Feynman gate is required for each flip-flop in the counter except the last one which requires one Feynman gate instead of double Feynman gate. So for n bit asynchronous counter it needs n Peres gate, (n-1) double Feynman gate and one Feynman gate. The quantum cost of double Feynman gate
is 2. So the total quantum cost is 4*n+2(n-1)+1 =6n-1, Hence Qn≥6n-1.

Theorem 3: To construct n (≥3) bit synchronous counter, if g is the total number of gates required to design the counter producing b number of garbage outputs then g≥4n-4 and b≥n.
Proof: Each flip-flop consists of two gates; n bit counter requires n number of flip-flops. For n=3, one Toffoli and one Feynman is required to carry out all the outputs to the next higher positioned flip-flop. So total number of gates required is 3*2+2=8.
For n>3, 2n number of gates required for the flip-flops and 2(n-2) number of gates are required to carry out all the lower outputs to the next higher outputs. So the total number of gates required is 2n+2(n-2)=4n-4. Every flip-flop produces only one garbage output. No garbage output produced while interconnection among flip-flops and to carry out outputs to next higher flip-flop. So the total number of garbage out is n, hence b≥n.

Theorem 4: The quantum cost of an n(≥3) bit synchronous counter is Qn≥11n-12.
Proof: For n (≥3) bit synchronous counter it requires n flip-flops. Each flip-flop consists of one Peres gate and one Feynman gate. Additional (n-2) Toffoli gates and (n-2) Feynman gates are required to carry out all the outputs to the next higher flip-flop. So it requires n number of Peres gate, (n-2) number of Toffoli gates and n+(n-2) =2n-2 number of Feynman gates. Quantum cost of Peres gate is 4, Quantum cost of Toffoli gate is 5 and quantum cost of Feynman gate is 1. So total quantum cost = 4*n + 5*(n-2)+1*(2n-2)=11n-12, hence Qn ≥11n-12.

APPLICATION
Since reversible logic has the potential to dissipate no heat at ideal condition and power dissipation is less when compared to irreversible logic, reversible computing may have applications in computer security and transaction processing, but the main long-term benefit will be felt very well in those areas which require high energy efficiency,speed and performance. It include the area like low power CMOS, quantum computer, nanotechnology, optical computing, design of low power arithmetic and data path for digital signal processing (DSP), Field Programmable GateArrays (FPGAs) in CMOS technology for extremely low power, high testability and self-repair.

PROPOSED SYSTEM
BLOCK DIAGRAM

Figure_7 SMBD Gate

RTL Schematic of Cyclic Gray Code Counter

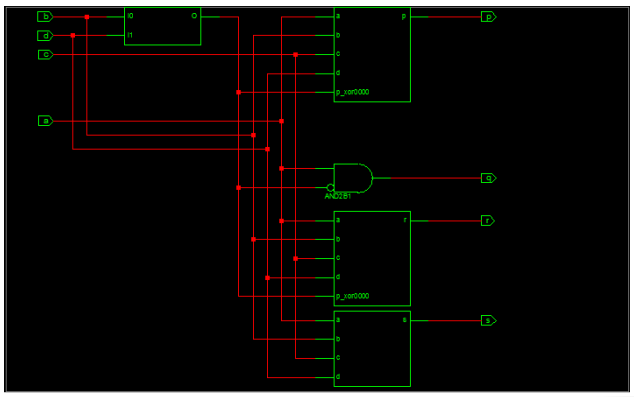

Figure_8 4 bit SGCCC

EXPLANATION:

SYNCHRONOUS GRAY CODE CYCLIC CODE COUNTER

Gray code was invented by Frank Gray.in 1953.It was earlier described in 1947. During the year 1930 & 1940, Gray was a researcher at bell telephone laboratories. According to Hesath used bu BAuDOT in 1870,it became widely popular. Gray code is otherwise known as “single distance code”.

Definition of Gray Code

Gray had interest in analog to digital conversion. The main aim is to convert an integer value,series of pulses in to digital form. Th e conversion of voltage todisplace vertically an electron beam swept across thecathode ray tube. The screen is mak etched, a current is generated when the beam passes through it.Then it gives a series of ON/OFF conditions.

There is a problem in this case. A distortion arises when a beam is close to the boundary.

PROPERTY OF GRAY

Property p1:

Adjacent words in the gray code sequence differ in one bit position only.

Property p2:

The Gray code is cyclic. These two properties are the two most common properties. So the Gray code has another apparent advantage that The pattern was reprinted

RESULT

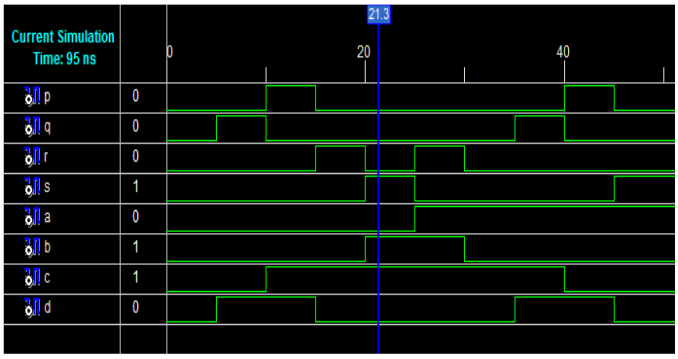

Figure_9 Simulated Output for 4 bit SGCCC

This is the simulated output for 4 bit Synchronous Gray Code Cyclic code Counter.It is simulated through XiLinx ISE 9.2 simulator.

CONCLUSION

In this paper a new reversible gate SMBD has been proposed. Appropriate algorithms and theorems are presented to clarify the proposed design and to establish its efficiency. As compared to the best reported designs in literature, the proposed designs are better in terms of delay,complexity & cost.Thus for future research,efficient design schemes for reversible more complex sequential circuit is an interesting area to investigate.

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