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Optimization using Partially Polar Encoder Architecture for Long Polar codes

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***Abstract*—Polar codes have emerged as important error correction codes due to their capacity achieving property. Successive cancellation (SC) algorithm is viewed as a good candidate for hardware design of polar decoders due to its low complexity. Although the previous fully parallel encoder is intuitive and easy to implement, it is not suitable for long polar codes because of the huge hardware complexity required. The Partial parallel encoder is intuitive and easy to implement, it is not suitable for long polar codes because of the huge hardware complexity required. The partial parallel encoder architecture that is adequate for long polar codes but increases in delay. The proposed architecture is used to avoid the faulty outputs in the propagation path of encoder circuit and delay element is added in each and every stage to get fault free output. In this brief, we analyze the encoding process in the viewpoint of very-large-scale integration implementation and simulation result shows the reduction in faulty output.**

Keywords*—component; formatting; style; styling; insert (key words)

I. INTRODUCTION

Polar Codes [1] are the first error-correcting codes with an explicit construction to provably achieve the symmetric capacity of memory-less channels. Since their introduction in 2008, polar codes have attracted a lot of attention from the information theory community, as they are the first codes to provably achieve channel capacity, asymptotically in code length. These linear block codes are proven to achieve the capacity of any symmetric memory-less channel under successive cancellation (SC) decoding [2]. To date, many efforts have addressed several theoretical aspects of polar codes including code construction and decoding algorithms, have been investigated in previous works [1]-[5], and efficient decoding structures have been studied.

On the other hand, hardware architecture for polar encoding have rarely been discussed. Among a few manuscripts dealing with hardware implementation, [1] presented a straight forward encoding architecture that processes all the message bits in a fully parallel manner. The fully parallel architecture is intuitive and easy to implement, but it is not suitable for long polar codes due to excessive hardware complexity. In addition, the partial sum network (PSN) for an SC decoder [7], [8], [11] is regarded as a polar encoder. Due to the nature of successive decoding, however the number of inputs is severely restricted in the PSN, 1 or 2 bits at a time. Christo Ananth et al. [12] proposed a system in which the complex parallelism technique is used to involve the processing of Substitution Byte, Shift Row, Mix Column and Add Round Key. Using S- Box complex parallelism, the original text is converted into cipher text. From that, we have achieved a 96% energy efficiency in Complex Parallelism Encryption technique and recovering the delay 232 ns. The complex parallelism that merge with parallel mix column and the one task one processor techniques are used. In future, Complex Parallelism single loop technique is used for recovering the original message.

II. POLAR ENCODING

In this section, a partially parallel encoder structure are designed to encode long polar codes efficiently. To clearly show the partially parallel encoder and how to transform the architecture, a 4-parallel encoding architecture for the 16-bit polar code is exemplified in depth. The fully parallel encoding architecture is first transformed to a folded form [15], [18], and then the lifetime analysis [16] and register allocation [17] are applied to the folded architecture. Lastly, the proposed parallel architecture for long polar codes is described.

A straightforward fully parallel encoding architecture was presented in [1], which has encoding complexity of O (N log N) for a polar code of length N and takes n stages when N=2 n. For example, a polar code with a length of 16 is implemented with 32 XOR gates and processed with four stages, as depicted in Fig.1

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This architecture continuously processes four samples per cycle according to the folding sets and the register allocation table. Note that the proposed encoder takes a pair of inputs in a natural order and generates a pair of outputs in a bit reversed order.

As the functional unit in the proposed architecture processes a pair of 2 bits at a time, the proposed architecture maintains the consecutive order at the input side and the bit reversed order at the output side if a pair of consecutive bits is regarded as a single entity.

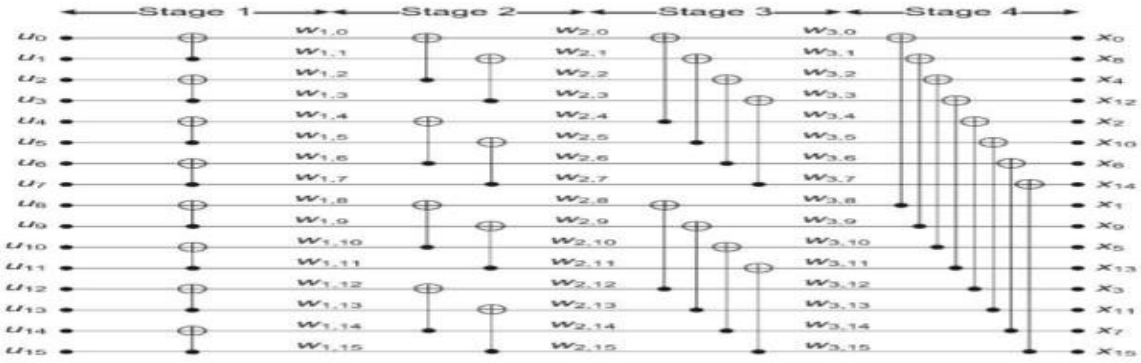

Fig1: Fully Parallel architecture for encoding a 16-bit polar code

This brief has presented a new partially parallel encoder architecture developed foe long polar codes . Many optimization techniques have been applied to derive the proposed architecture . Experimental results show that the architecture can save the hardware compared with that of the fully parallel architecture . Finally , the relationship between the hardware complexity and the throughputs is analyzed to select the most suitable architecture for a given application . therefore , this architecture provides a practical solution for encoding a long polar code.

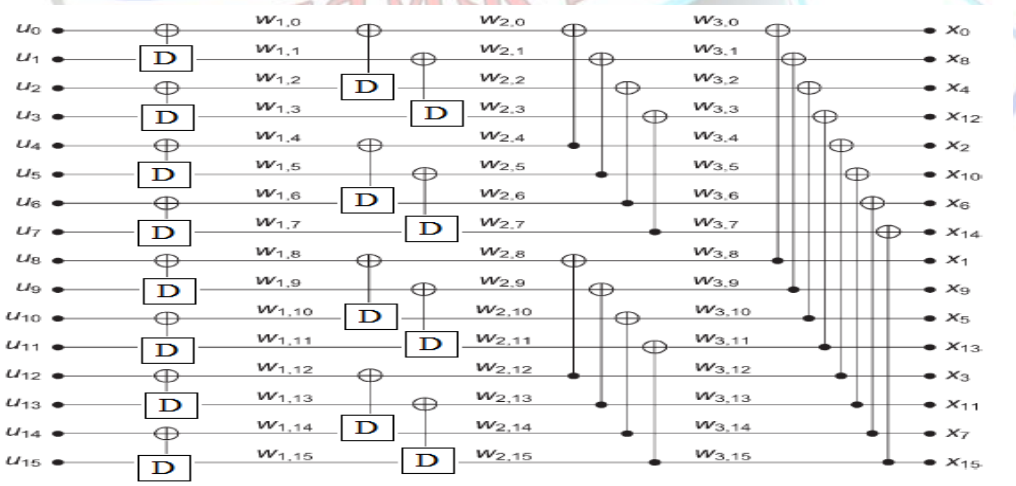

Fig2: Proposed parallel architecture for encoding a 16-bit polar code using delay element

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PARALLELISM	16BIT		32BIT		64BIT	
	EXISTING	PROPOSED	EXISTING	PROPOSED	EXISTING	PROPOSED
SLICES	18	13	36	26	72	52
LUT	20	16	40	32	80	64
NO. OF SLICES(FLIP FLOP)	32	21	64	42	128	84

III. PROPOSED POLAR ENCODER

The Proposed parallel architecture for encoding a 16- bit polar code using delay element is shown in fig 2 . The retiming is a transformation technique used to change the locations of delay element in a circuit without affecting the input/output.

Characteristics of the circuit. Critical path is defined to be the path with the longest computation time among all paths that contain zero delay. The lower bound on the clock period of the circuit can be achieved by retiming.

The proposed architecture is used to avoid the faulty outputs in the propagation path of encoder circuit and delay element is added in each and every stage to get fault free output. In order to avoid faulty outputs in the propagation path of encoder we retime by cutest retiming in above proposed block diagram each and every stages delay element is added to get fault free outputs. In practical implementations, the memory size and the number of XOR gates increase as the code length increases.

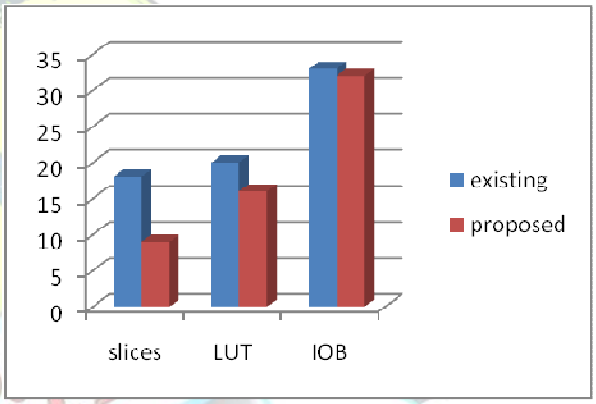

Fig.3: Performance measure of existing and proposed

IV. SIMULATION RESULT

The proposed has been simulated and the synthesis report can be obtained by using Xilinx ISE 12.1 simulator. The various parameters used for computing existing and proposed systems with Spartan-3 processor are given in the table 1.

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From the synsthesized results, it is found that the Proposed sysem is reduced in Slices, LUT and Number of Slice flip flop as compared with the existing system.

The Figure 4 shown that there is a considerable reduction in time and area based on the implementation results which have been done by using Spartan-3 processor. The proposed algorithm significantly reduces area consumption when compared to the existing system.

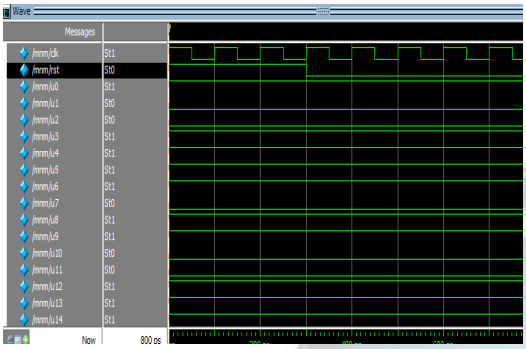

Fig4: Simulation result for Proposed system

V. CONCLUSION

This brief has presented a new partially parallel encoder architecture with retiming developed for long polar codes. By cut-set retiming we have been able to reduce the critical path to one XOR gate delay. Many optimization techniques have been applied to derive the proposed architecture. Proposed architecture gives glitch free outputs without adding additional delay in propagation path. Therefore, the proposed architecture provides a practical solution for encoding a long polar code.

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