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PFC BRIDGELESS SEPIC CONVERTER-FED BLDC MOTOR DRIVE

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ABSTRACT-*This paper deals with power factor correction based SEPIC converter fed brushless dc motor drive as a cost effective solution for low power applications. The speed of the brushless dc motor is controlled by varying the dc pulse voltage of a voltage source inverter which uses a low frequency switching of voltage source inverter for low switching losses. A SEPIC converter working in a discontinuous conduction mode is used for control of dc link voltage with an unity power factor at AC mains. Performance of the power factor correction SEPIC converter is evaluated under four different operating conditions of discontinuous conduction mode and a comparison is made to select the best suited mode of operation. The performance of the proposed system is simulated in a matlab/simulink environment and hardware prototype of the proposed drive is developed to validate its performance over a wide range of speed with unity power factor at AC mains.*

Keywords: BLDC MOTOR, VSI (Voltage Source Inverter), SEPIC Converter, MATLAB.

I. INTRODUCTION

The BLDC motor is a three-phase synchronous motor consisting of a stator having a three-phase concentrated windings and a rotor having permanent magnets. It does not have mechanical brushes and commutator assembly; hence wear and tear of the brushes and sparking issues as in case of conventional dc machines are eliminated in BLDC motor and thus it has low EMI problems. This motor is also referred as an electronically commutated motor since an electronic commutation based on the Hall-effect rotor position signals is used rather than a mechanical commutation. The conventional scheme of a BLDC motor fed by a diode bridge rectifier (DBR) and a high value of dc-link capacitor draws a non sinusoidal current, from ac mains which is rich in harmonics such that the THD of supply current is as high as 65%, which results in PF as low as 0.8. Most of the PMBLDC drive from the supply via diode bridge rectifier and a capacitor. But the capacitor draws pulsated currents which results in harmonics due to an uncontrolled charging of the dc link capacitor. So PFC converters are implemented in front of the dc link capacitor in order to supply a constant DC current. Therefore, a PF correction (PFC) converter among various available converter topologies [3] is applicable for a PMBLDCMD. Among these topologies most of them use boost topology at them front end. But the switching losses are high due to the presence o f the diode bridge. This affects the efficiency of the whole drive system. Several topologies are proposed in order to maximize the efficiency of power supply. Bridgeless topologies are one such converter which can reduce the switching losses by reducing the number of power semiconductor switches in the current conduction path. By using this bridgeless

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topology the input diode bridge is avoided and therefore conduction losses are reduced which yield a better efficient system. Mostly used converter topology is bridgeless boost converter. But it is applicable only for boost operation and moreover it has high start up inrush current and lack of galvanic isolation. The topology which introduces a buck bridgeless converter has the disadvantages like low output voltage, high output voltage ripple. By using this bridgeless topology the input diode bridge is avoided and therefore conduction losses are reduced which yield a better efficient system. Mostly used converter topology is bridgeless boost converter. But it is applicable only for boost operation and moreover it has high start up inrush current and lack of galvanic isolation. The topology of CUK converter has relatively high output ripple due to the discontinuous and continuous output current. So if these converters are used in a drive system disadvantages of those converters will decrease the efficiency of the whole drive system. The SEPIC topology based converter offer various advantages ahead of the above topologies, such as lower input current ripple, low switching losses, and has low harmonics associated with the discontinuous conduction mode (DCM) topology. Hence, single-phase power factor correction (PFC) converters are used to attain a unity PF at ac mains. These converters have gained attention due to single-stage requirement for dc-link voltage control with unity PF at ac mains. It also has low component count as compared to a multistage converter and therefore offers reduced losses.

II. CONCEPT OF SEPIC CONVERTER

In DC-DC converters the SEPIC topology is a lesser known relative of the Cuk topology. But this converter provide a positive output voltage that can be greater than, equal to or less than VIN while avoiding the complexity and cost of a buck-boost converter.

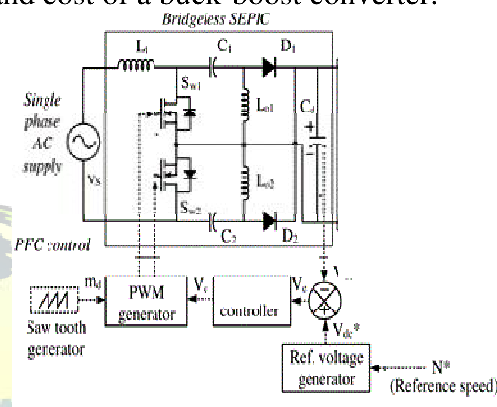

Fig.1: Block Diagram of SEPIC Converter.

The SEPIC converter has the advantage such as which minimize a ripple current, produce high efficiency, reduces the harmonics and switching losses.

III. PFC SEPIC CONVERTER –FED BLDC MOTOR DRIVE

Single stage PFC converters have gained importance due to simplicity in design and low amount of losses due to less count of components.The bridgeless SEPIC converter is used to control the DC-link voltage (Vdc) of the VSI and to achieve a unity power factor at AC mains.

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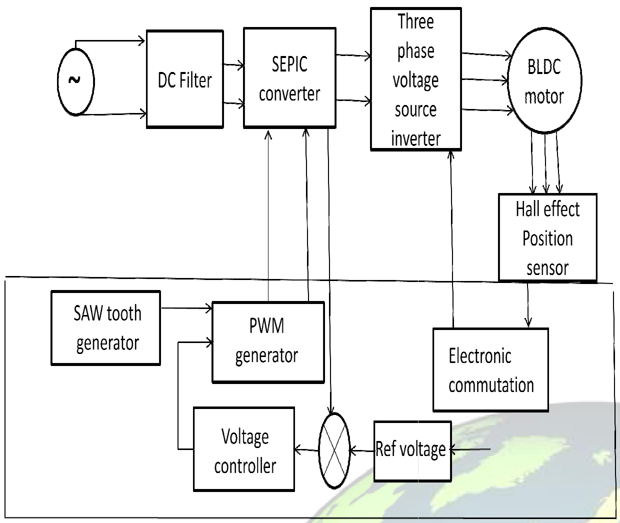

Fig. 2: Block Diagram of PFC SEPIC Converter –fed BLDC Motor

Fig. 2 shows the PFC SEPIC converter-based VSI-fed BLDC motor drive using a current multiplier and a voltage follower approach,respectively.Here a high frequency metal–oxide– semiconductor field-effect transistor (MOSFET) is used in the SEPIC converter for PFC and voltage control , whereas insulated-gate bi polar transistors(IGBTs) are used in the VSI for its low frequency operation. The BLDC motor is commutated electronically to operate the IGBTs of VSI in fundamental frequency switching mode to reduce its switching losses.

Single stage isolated PFC converters provides isolation between input and output. Bridgeless converters have gained importance due to elimination of DBR at the input which consequently reduce the conduction losses of diodes and thus improve the overall efficiency of the converter. Elimination of two diodes or complete elimination of diodes in a DBR depend support configuration of the converter.

A new approach of speed control by controlling the voltage at the DC link is used which utilizes a fundamental frequency switching of VSI (i.e. electronic commutation of BLDC motor) hence offers reduced switching losses. A voltage follower approach is used for the control of bridgeless SEPIC converter operating in discontinuous inductor current mode (DICM) in which a single voltage sensor is required for the sensing of DC-link voltage (Vdc).

A bridgeless topology utilizing Zeta and Cuk converter have been widely used for the development of the PFC converter with improved power quality at the AC mains .An isolated SEPIC converter operating in CCM (Continuous Conduction Mode) or DCM (Discontinuous Conduction Mode) is widely used for PFC applications . DCM is preferred for low and medium power applications because it utilizes an approach of voltage follower which requires a single voltage sensor for DC link voltage control and PFC operation.

IV. SYSTEM CONFIGURATIONS

CCM uses a current multiplier technique, which requires three sensors (one current and two voltage sensors) for operation and thus increases the overall cost of drive system. This paper explores the potential of SEPIC converter for BLDC motor drive targeting special class of applications.

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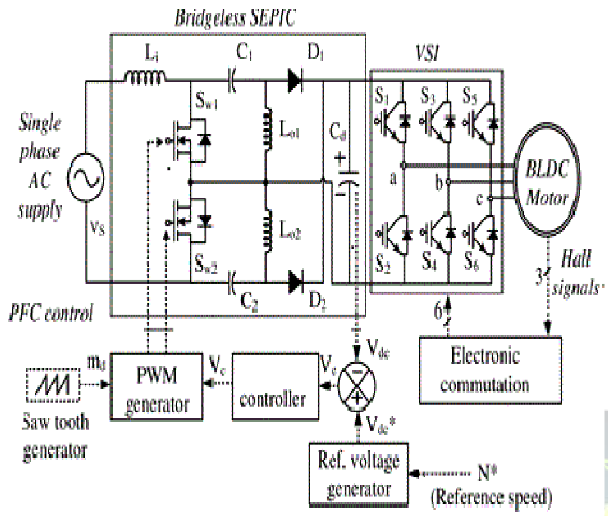

Fig.3: Bridgeless SEPIC Converter fed BLDC Motor Drive

Moreover, possibilities of employing a bridgeless configuration in SEPIC converter are still unexplored. The drive system is needed to be developed which must incorporate features like low cost, high efficiency and satisfactory performance with improved power quality at the AC mains for a wide range of speed control. This work is targeted to achieve all these objectives in the proposed drive.

V. PRINCIPLE OF OPERATION OF BRIDGELESS SEPIC CONVERTER

A bridgeless topology is designed such that two switches conduct independently for the positive and negative half cycle of the supply voltage. The conduction losses of the DBR are reduced to half as compared to conventional topology due to the bridgeless configuration**.** Moreover, this also improves the thermal utilization of switches since switch rms current is divided into two switches.

i) Operation during Complete Cycle of Supply Voltage:

In this switch Sw1 and diode D1 (fig.3) conduct for the positive half cycle of the supply voltage and diode D2 remains reversed biased during this period. Similarly for the negative half cycle of the supply voltage, switch Sw2 and diode D2 conduct and no current flows through switch Sw1 and diode D1.

The energy is transferred through all the components. The magnetizing inductance (Lm) is designed to operate in DCM such that a discontinuous conduction is achieved for a wide range of DC link voltage control to achieve an inherent power factor correction.

ii) Operation during Complete Switching Cycle:

In this switch Sw1 is on (Fig.3), the energy is stored in the intermediate capacitor C1 and inductor Lo; whereas DC link capacitor Cd supplies the required energy to the load. When switch is turned off, the energy discharges through Diode D and inductor Lo supplies the required energy to the DC link capacitor.

In the DCM mode the energys is completely discharged, whereas inductor Lo continues to supply the required energy to the DC link capacitor.

VI. CONTROL OF BLDC MOTOR ELECTRONIC COMMUTATION

An electronic commutation of the BLDC motor includes the proper switching of VSI in such a way that a symmetrical dc current is drawn from the dc link capacitor for 120◦ and placed symmetrically at the centre of

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each phase. A Hall-effect position sensor is used to sense the rotor position on a span of 60◦, which is required for the electronic commutation of the BLDC motor.

The conduction states of two switches (S1 and S4) are shown in Fig. 4. A line current iab is drawn from the dc link capacitor, whose magnitude depends on the applied dc link voltage (Vdc),Back electromotive forces (EMFs) (ean and ebn), resistances (Ra and Rb), and self inductance and mutual inductance (La, Lb, and M) of the stator windings. Table II shows the different switching states of the VSI feeding a BLDC motor based on the Hall-effect position signals (Ha – Hc).

VII. SIMULATION CIRCUIT OF PFC BRIDGELESS SEPIC CONVERTER FED BLDC MOTOR DRIVE

BL SEPIC is a dc-dc converter similar to BL buck-boost the below shown fig 5 &5.1 represents the matlab simulation circuit of PFC BL SEPIC converter fed BLDC motor drive. In this circuit shows the performance of BLDC motor, speed is directly proportional to voltage of dc link capacitor. VSI (voltage source inverter) is used to supply the voltage to the motor by means of electronic commutation. In frontend the BL SEPIC converter is operated as both PFC and ac-dc converter.

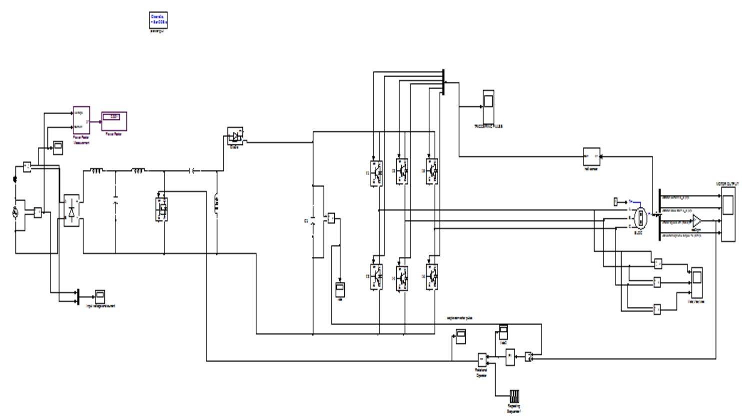

Fig.5: Simulation Circuit of PFC SEPIC Converter

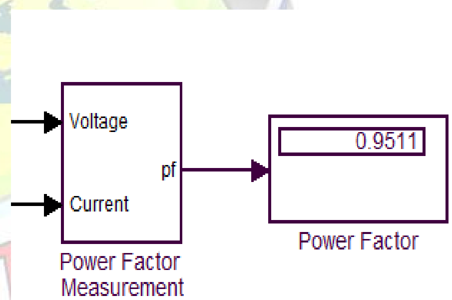

Fig.5.1: Power Factor at Speed 1200 RPM

The switches s1 and s2 of BL SEPIC converter are operated independently for positive and negative half cycles of supply voltage. Then the output voltage of SEPIC converter is greater than or less then to input voltage. The speed control of BLDC motor is obtained by voltage follower approach. As per our speed requirement the output voltage of BL SEPIC converter is changed. By sensing the output voltage of the BL SEPIC converter and comparing with reference voltage, then remaining voltage is again fed to switches by using the PWM technique. By this speed control of motor the performance of the converter can be achieved.

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IX. SIMULATED PERFORMANCE OF BLDC MOTOR DRIVE USING PFC BL SEPIC CONVERTER

The performance evaluation of BLDC motor drive is categorized in terms of the performance of the BLDC motor and BL SEPIC converter and achived power quality indices at ac mains.The parameters such as speed (N),torque (Te), source voltage(Vs),source current (Is) are determined, and demonstated in a proper funtioning of BLDC motor.

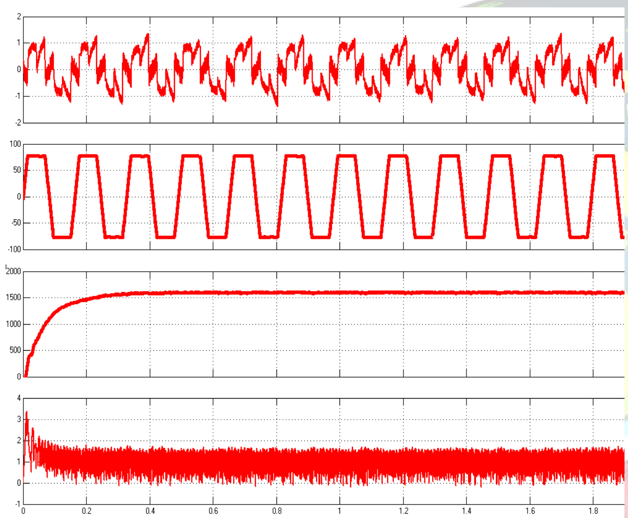

Fig.5: Steady- State Performance of BLDC Motor at Rated Condition

5.5 % THD Values of Source Current (I_s) in Bridgeless SEPIC Converter

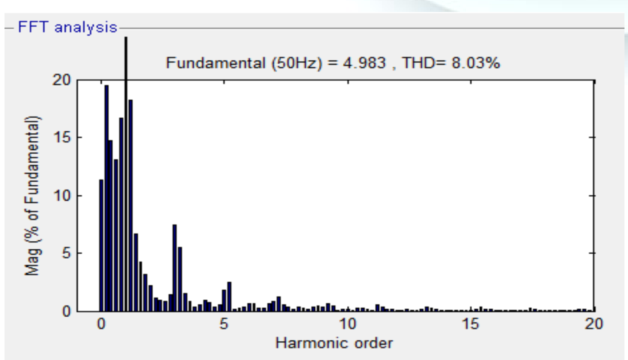

Fig.6: Harmonic Spectra of Supply Current at Rated Supply Voltage and Rated Loading on BLDC Motor for a DC Link Voltage of (a) 200v(BL SEPIC)

5.6 % THD Values of Source Current (Is) in BL SEPIC Converter

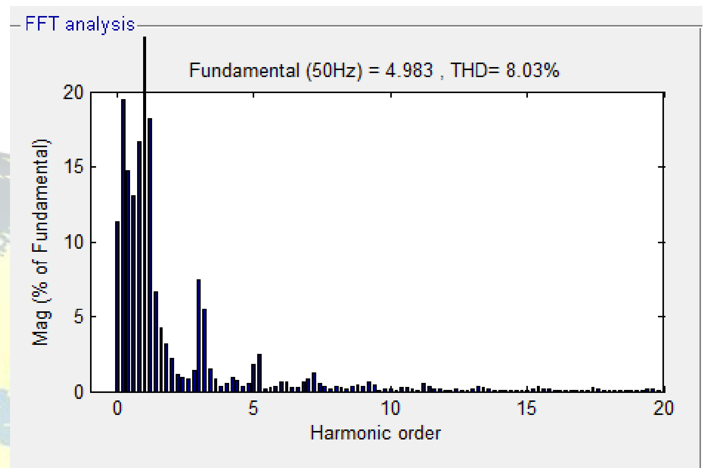

Fig.7: Harmonic Spectra of Supply Current at Rated Supply Voltage and Rated Loading on BLDC Motor for a Dc Link Voltage of 70v and (BL SEPIC).

X. CONCLUSION

The performance and analysis of BLDC motor with BL SEPIC converter is an effective cost solution for low and medium power applications. A new method of speed control has been utilized by controlling the voltage at dc bus and operating the VSI at fundamental frequency for electronic commutation of BLDC motor for reducing switching losses. The performance of BLDC motor analysed by comparing with BL SEPIC converter fed BLDC motor drive. Power factor is almost same in topologies. The transient and ripple content of output wave forms decreases in BL SEPIC converter topology.

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REFERENCES

[1] *T. K. A. Brekken, H. M. Hapke, C. Stillinger, and J. Prudell,* "Machines and drives comparison for low-power renewable energy and oscillating applications," IEEE Trans. Energy Convers., vol. 25, no. 4, pp. 1162–1170, Dec. 2010.

[2] *T. Y. Ho, M. S. Chen, L. H. Yang, and W. L. Lin,* "The design of a high power factor brushless DC motor drive*," in Proc. Int. Symp. Comput.Consum. Contr., Jun. 4–6, 2012, pp. 345–348.*

[3] *V. Bist and B. Singh*, "An adjustable speed PFC bridgeless buck-boost converter fed BLDC motor drive," *IEEE Trans. Ind. Electron., vol. 61,no. 6, pp. 2665–2677, Jun. 2014.*

[4] *B. Singh and V. Bist,* "An improved power quality bridgeless Cuk converter fed BLDC motor drive for air conditioning system," *IET Power Electron., vol. 6, no. 5, pp. 902–913, 2013.*

[5] PFC cuk converter fed BLDC motor drive, *Vashist bist, student member, IEEE, and bhim singh, fellow, IEEE; IEEE Transactions on power electronics, Vol. 30, no. february 2015.*

[6] *V. Bist and B. Singh*, "A reduced sensor PFC BL-zeta converter basedVSI fed BLDC motor drive," *Elect. Power Syst. Res., vol. 98, pp. 11–18,May 2013*.

[7] *N. Mohan, T. M. Undeland, and W. P. Robbins*, Power Electronics: Converters, Applications and Design. *New York, NY, USA: Wiley, 2009.*

[8] *C. L. Xia*, Permanent Magnet Brushless DC Motor Drives and Controls. *Beijing, China: Wiley, 2012.*

[9] *T. K. A. Brekken, H. M. Hapke, C. Stillinger, and J. Prudell*, "Machines and drives comparison for low-power renewable energy and oscillating applications," *IEEE Trans. Energy Convers., vol. 25, no. 4, pp. 1162–1170, Dec. 2010.*

[10] *L. Malesani, R. G. Spiazzi, and P. Tenti,* "Performance optimization of Cuk converters by sliding-mode control," *IEEE Trans. Power Electron.*, vol. 10, no. 3, pp. 302–309, May 1995.