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DESIGN OF LOW POWER CAM CELL ARRAY LOGIC WITH DISTANCE BASED SENSE AMPLIFIER

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***Abstract*—Content Addressable Memory (CAM) used in certain very high speed searching applications is a special type of computer memory. It is an associative storage, associative or associative array though this term associative array is generally used for a programming data structure. The proposed architecture is a CAM cell array with distance based sense amplifier. In this project, the system proposed an XOR based Content Addressable Memory. Distance based Sense Amplifier performs ML process based on XOR operation. In proposed system, reducing the delay time and to increase speed in ML process.**

***Index Terms*—Content Addressable Memory (CAM), Match line (ML), distance based sense amplifier.**

I. INTRODUCTION

The term "memory", defines "main memory" or "primary storage", is associated with addressable semiconductor memory, i.e. integrated circuits consisting of silicon-based transistors and used for example as primary storage but also other purposes in computers, other electronic devices. There are many types of semiconductor memory, volatile and nonvolatile. Examples of nonvolatile memory are flash memory, ROM, PROM, EPROM and EEPROM memory. Examples of volatile memory are primary storage and CPU cache memory [3]. Memory devices store and retrieve data by addressing specific memory locations. This path becomes controlling factor for systems that rely on fast memory accesses. The time to find the item stored in memory can be reduced considerably if that item can be identified for access by its content rather than by its address. A memory that is accessed in this way is known as CAM or content-addressable memory. CAM gives a performance advantage over other memory search algorithms, such as tree-based searches or binary or look-aside tag buffers, by comparing desired information against the total list of pre-stored entries simultaneously, resulting in an order-of-magnitude reduction in the search time. CAM is suited for many functions such as data compression, Ethernet address lookup, pattern-recognition, cache tags, fast lookup of routing, high-bandwidth address filtering, user privilege and security or encryption

Information for high-performance data switches, firewalls, bridges and routers [2].

Since CAM is an outgrowth of RAM technology in order to understand CAM, it helps to contrast with RAM. A RAM stores data temporarily. Data stored in a RAM at a appropriate location called an address. In a RAM, we supplies the Address and gets back the data. The address lines restrict the depth of memory using RAM, but we can extend the width of the memory as far as desired. With CAM, we supply the data and gets back the address. The CAM researches through the memory in one clock cycle, returns the address where the data is found. CAM can be preloaded at device startup and also be rewritten during device operation. Christo Ananth et al. [5] proposed a system, Low Voltage Differential Signaling (LVDS) is a way to communicate data using a very low voltage swing (about 350mV) differentially over two PCB traces. It deals about the analysis and design of a low power, low noise and high speed comparator for a high performance Low Voltage Differential Signaling (LVDS) Receiver. The circuit of a Conventional Double Tail Latch Type Comparator is modified for the purpose of low-power and low noise operation even in small supply voltages. The circuit is simulated with 2V DC supply voltage, 350mV 500MHz sinusoidal input and 1GHz clock frequency. LVDS Receiver using comparator as its second stage is designed and simulated in Cadence Virtuoso Analog Design Environment using GPDK 180nm .By this design, the power dissipation, delay and noise can be reduced. The CAM can operate as a data-parallel or Single Instruction/Multiple Data processor [8].

This brief is organized as follows. Section II illustrates the system architecture. Section III describes Proposed RAM-CAM architecture design. The conclusions are given in Section IV.

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II.SYSTEM ARCHITECTURE

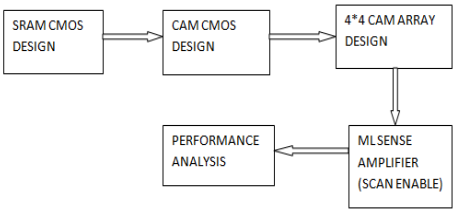

Fig1: Architecture Diagram

In Fig1, first of all the system design the 6T based SRAM CMOS design. This design is to store the single bit value. This design consists of two inverter cross connection to maintain the given input data. Then the system designs the 8T-XOR CAM CMOS design. It consists of Selection line and the bit line to control the CAM cell. This process used to find the address bit location.

Then the scan based enable process is to find the CAM cell array result. The XOR-gate function to match the SRAM data and CAM data and to invert the activation result. The match line process is to check the cam data register. The clock function is to control the output matched line row then it will get the content address.

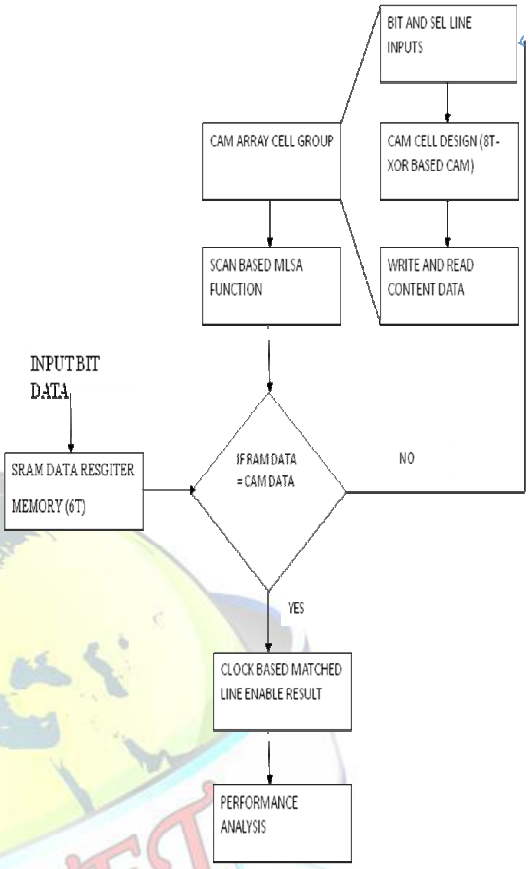

Fig 2: Flow chart of Proposed CAM

In Fig 2, the input data is given to SRAM. The SRAM starts checking process. It checks whether the RAM data is equal to CAM data. If both the data are equal and we observe 'yes' in the flow diagram, the checking process stops by the clock based matched line enable result and get the output. Then it is given to the performance analysis. It identifies the content address effective one. It considers the power consumption level. It checks ML delay time. If the RAM data and CAM data are not equal then we can observe 'No' in this diagram.

If No occurs, then the input bit will go to CAM array cell group. It has Bit and SEL line inputs, CAM cell design (8T XOR based CAM), Write and read content data. The Bit line provides the data and SEL line Controls the match line. SEL line checks if its input is matched to the CAM storage data in CAM cell design. Then it reads and writes content data. Then it is given to Scan based MLSA function. It acts as a content retriever.

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III. RAM-CAM ARCHITECTURE DESIGN

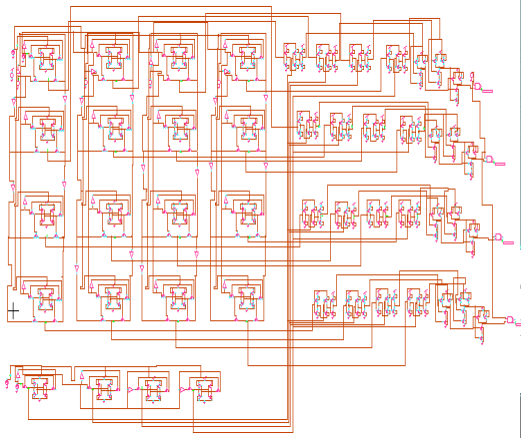

Fig 3: Schematic diagram of RAM-CAM

The above figure consists of 4*4 CAM array design, SRAM CMOS design, Distance based sense amplifier, and clock. The clock function is to control the output matched line row and to get the content address. In this design using distance based sense amplifier XOR operation is done on the search and stored words and then its result is used to check whether the search and stored words is same or different.

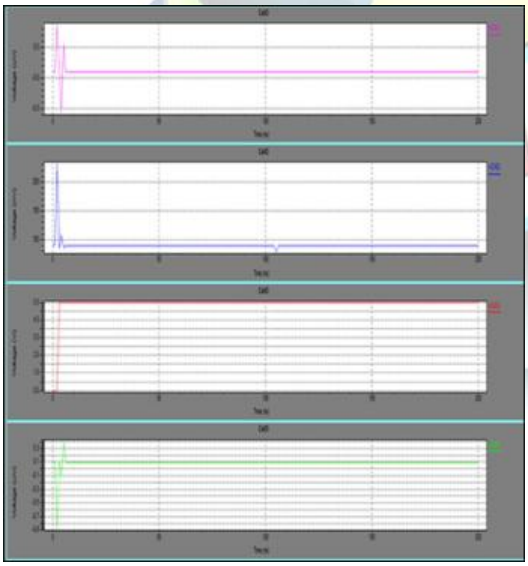

Fig 4: Simulation results for RAM-CAM

In the Fig 4, the output waveform has a match line of the given 4 bit word and it shows the CAM third row is matching. Then to export the circuit files to find power and delay measurement.

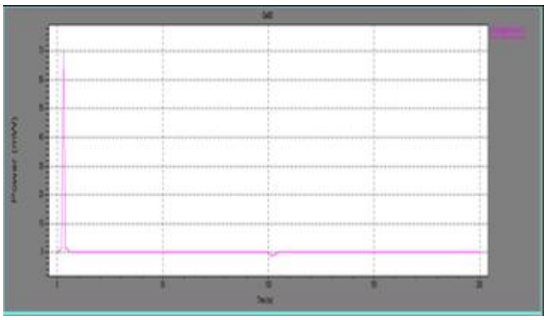

Fig 5: Power Measurement

The above diagram shows the total estimated power consumption of 70mW. Our proposed system power consumption is lesser than existing system.

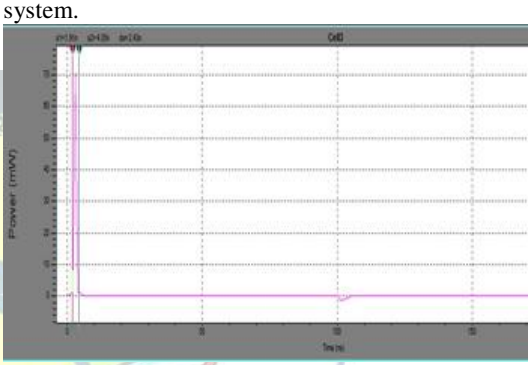

Fig 6: Delay Measurement

In the above figure, the delay time is measured. The delay time of the proposed system is 2.2ns. It is lesser than the existing system whose value is 7ns.

Table I
RESULT COMPARISONS

Parameters	SCN-CAM	RAM-CAM
AREA	4.83mm^2	0.320mm^2
POWER	94mW	70Mw
DELAY TIME	7ns	2.2ns

Table I summarizes the comparisons of the area, delay time and power consumption between SCN-CAM and RAM-CAM.

IV. CONCLUSION

In this paper, a XOR based Content Addressable Memory has been presented. It is a very low power CAM cell. CAM is suitable for low-power applications, where frequent and parallel look-up operations are needed. In a conventional CAM array, each entry consists of a

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tag, if it is matched with the input, points to the place of a data word in a static random access memory block. The actual data of interest are stored in SRAM and a tag is commonly a reference to it. Therefore, when it is required to search for the data in SRAM, it is enough to search for its corresponding tag. Therefore, the tag is shorter than the SRAM data and would need fewer bit comparisons. Achieves simple and fast updates can be achieved without retraining the network entirely. Depending on the application, non-uniform inputs may result in higher power consumption, but does not affect the accuracy of the final result.

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