ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 3, Special Issue 2, March 2016

AREA EFFICIENT Z-TCAM BY USING SRAM BASED ARCHITECTURE FOR TCAM

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ABSTRACT—

Content Addressable Memory (CAM) offers high-speed search function in a single clock cycle. Due to its parallel match-line comparison, CAM is power-hungry. Thus, robust, high-speed and low-power sense amplifiers are highly sought-after in cam designs.In This Paper, a novel memory architecture called Z-TCAM. It is implemented by TCAM function with SRAM. Z-TCAM Logically partitions the classical TCAM table along colomns rows into hybrid TCAM subtables, it is processed to map on their corresponding memory blocks. Z-TCAM is implemented by using Xilinx Virtex-7 FPGA.The proposed Z-TCAM offers comparable Search performance and Lower cost than Classical TCAM devices.

Index Terms — Application-specificintegratedcircuit(ASIC), field-programmablegate array (FPGA),memory architecture, priority encoder,staticrandom accessmemory(SRAM)-based TCAM,ternarycontentaddressablememory(TCAM).

I.INTRODUCTION

CAM stands for Content Addressable Memory which is a special type of memory used by Cisco switches. In the case of ordinary RAM the IOS uses a memory address to get the data stored at this memory location, while with CAM the IOS does the inverse. It uses the data and the CAM returns the address where the data is stored. Also the CAM is considered to be faster than the RAM since the CAM searches the entire memory in one operation.CAM tables provide only two results: 0 (true) or 1 (false).

TCAM stands for Ternary Content Addressable Memory is the capability extension of CAM which can match a third state, which is any value. This makes TCAM a very important component of Cisco Layer 3 switches and modern routers, since they can store their routing table in the TCAMs, allowing for very fast lookups, which is considerably better than routing tables stored in ordinary RAM. TCAM is a specialized CAM designed for rapid table lookups. TCAM A cell has two static random access memory (SRAM)

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cells and a comparison circuitry and provides three state: 0, 1, and x where x is a don't care state. The x state is always regarded as matched irrespective of the input bit. TCAM provides single clock lookup with constant search time which makes it suitable for applications such as network routers, data compression, real-time pattern matching in virus-detection, and image processing

TCAM is designed using SRAM which is called as Z-TCAM , because even though the TCAM table provides lookup of entire table in single clock it has various disadvantages when compared to SRAM.TCAM cells, comparator's circuitry in add complexity to the TCAM architecture. The access time of TCAM, is3.3 times longer than the SRAM access time due to the massive parallelism.

TCAM islessdensethanSRAM. Thecomparator's circuitry in TCAMcelladdscomplexitytotheTCAMarchitecture. Theextra logicandcapacitiveloadingduetothemassiveparallelism lengthen theaccesstimeofTCAM, whichis3.3timeslongerthantheSRAM accesstime[3].Inbornarchitectural barriersalsolimitthetotalchip capacityofTCAM.Complex integration ofmemoryandlogicalso makesTCAMtestingverytimeconsuming[1].

Furthermore,thecostofTCAMisabout30timesmoreperbit ofstoragethanSRAM[4].RAMisavailable inawidervarietyof sizesandflavors,ismoregenericandwidelyavailable,andenables to avoid the heavy licensing and royalty costs charged by some CAMvendors[5].CAMdeviceshaveverylimitedpatterncapacity

II.THE PROPOSED SCHEME

We introduce a versatile auxiliary bit to boost the search speed of the CAM at the cost of less than 1% area overhead and power consumption.This newly introduced auxiliary bit at a glance is similar to the existing *Pre-computation schemes* but in fact has a different operating principle.This Brief Proposes a novel memory architecture name is Z-TCAM.It Uses TCAM function with SRAM.Z-TCAM Logically partitions the classical TCAM table along colomns rows into hybrid TCAM subtables,it is processed to map on their corresponding memory blocks. Z-TCAM will implemented by using Xilinx Virtex-7 FPGA.The proposed Z-TCAM offers comparable Search performance,Lower cost than Classical TCAM devices.

A.Architecture Of Z-TCAM

Content Addressable memory (CAM) is a special type of computer memory used in certain very high speed searching applications. it is also known as associative memory, or associative array, although the last term is more often used

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for a programming data structure.[1] It compares input search data (tag) against a table of stored data, and returns the address of

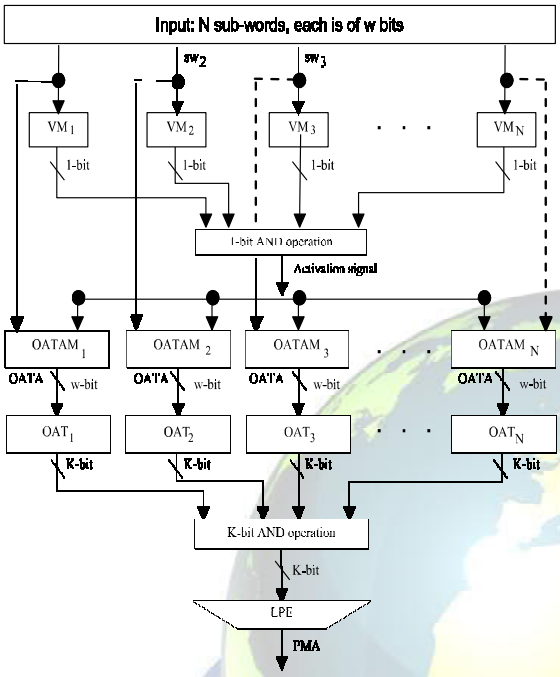

Fig 1 .ArchitectureofalayerofZ-TCAM

matching data (or in the case of associative memory, the matching data).[2] Several custom computers, like the Goodyear STARAN, were built to implement CAM, and were designated associative computer

B. Semiconductor Implementations:

Because a CAM is designed to search its entire memory in a single operation, it is much faster than RAM in virtually all search applications. There are cost disadvantages to CAM however. Unlike a RAM chip, which has simple storage cells, each individual memory bit in a fully parallel CAM must have its own associated comparison circuit to detect a match between the stored bit and the input bit. Additionally, match outputs from each cell in the data word must be combined to yield a complete data word match signal. The additional circuitry increases the physical size of the CAM chip which increases manufacturing cost. The extra circuitry also increases power dissipation since every comparison circuit is active on every clock cycle. Consequently, CAM is only used in specialized applications where searching speed cannot be accomplished using a less costly method. One successful early implementation was a General Purpose Associative Processor IC and System.

C.Binary CAM:

Binary CAM is the simplest type of CAM which uses data search words consisting entirely of 1s and 0s. Ternary CAM (TCAM)[7] allows a third matching state of "X" or "don't care" for one or more bits in the stored data word, thus adding flexibility to the search. For example, a ternary CAM might have a stored word of "10XX0" which will match any of the four search words "10000", "10010", "10100", or "10110". The added search flexibility comes at an additional cost over binary CAM as the internal memory cell must now encode three possible states instead of the two of binary CAM. This additional state is typically implemented by adding a mask bit ("care" or "don't care" bit) to every memory cell.

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D.Hardware Associate Array:

Unlike standard computer memory (random access memory or RAM) in which the user supplies a memory address and the RAM returns the data word stored at that address, a CAM is designed such that the usersupplies adata word and the CAM searches its entire memory to see if that data word is stored anywhere in it. If the data word is found, the CAM returns a list of one or more storage addresses where the word was found (and in some architectures, it also returns the data word, or other associated pieces of data). Thus, a CAM is the hardware embodiment of what in software terms would be called an associative array. The data word recognition unit was proposed by Dudley Allen Buck in 1955.[3] Holographic associative memory provides a mathematical model for "don't care" integrated associative recollection using complex valued representation.

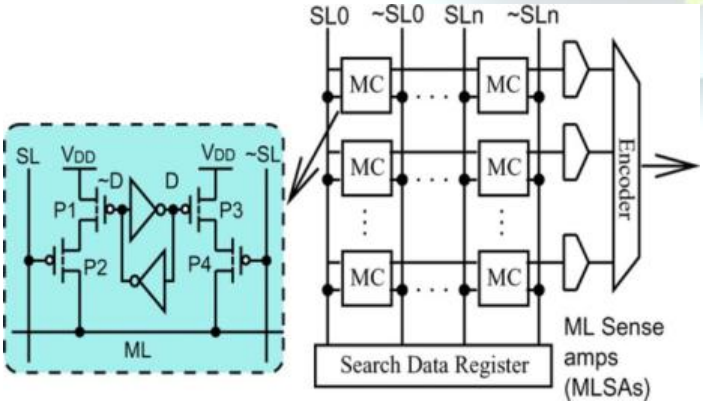

Fig2.Block diagram for conventional RAM

E. Proposed Auxillary Scheme:

1) Pre-Computation CAM Design: The pre-computation CAM uses additional bits to filter some mismatched CAM words before the actual comparison. These extra bits are derived from the data bits and are used as the first comparison stage. For example, in Fig. 2(a) number of "1" in the stored words are counted and kept in the Counting bits segment. When a search operation starts, number of "1"s in the search word is counted and stored to the segment on the left of Fig. 2(a). Christo Ananth et al. [11] proposed a system, Low Voltage Differential Signaling (LVDS) is a way to communicate data using a very low voltage swing (about 350mV) differentially over two PCB traces. It deals about the analysis and design of a low power, low noise and high speed comparator for a high performance Low Voltage Differential Signaling (LVDS) Receiver. The circuit of a Conventional Double Tail Latch Type Comparator is modified for the purpose of low-power and low noise operation even in small supply voltages. The circuit is simulated with 2V DC supply voltage, 350mV 500MHz sinusoidal input and 1GHz clock frequency. LVDS Receiver using comparator as its second stage is designed and simulated in Cadence Virtuoso Analog Design Environment using GPDK 180nm .By

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this design, the power dissipation, delay and noise can be reduced. Thus, we propose a new auxiliary bit that can concurrently boost the sensing speed of the M_L and at the same time improve of the M_LCAM by two times.

2) Parity Bit Based CAM:The parity bit based CAM design is shown in Fig. 2(b) consisting of the original data segment and an extra one-bit segment, derivedfrom theactual data bits. We only obtain the parity bit, i.e., odd or even number of "1"s. The obtained parity bit is placed directly to the corresponding word andthus the new architecture has the same interface as the conventional CAM with one extra bit. During the search operation, there is only one single stage as in conventional CAM. Hence, the use of this parity bits does not improve the power performance.However, this additional parity bit, in theory, reduces the sensing delay and boosts the driving strength of the 1-mismatch case (which is the worst case) by half, as discussed below.In the case of a matched in the data segment the parity bits of the search and the stored word is the same, thus the overall word returns a match. When 1 mismatch occurs in the data segment numbers of "1"s in the stored and search word must be different by 1. As a result, the corresponding parity bits are different.Therefore now we have two mismatches (one from the parity bit and one from the data bits). If there are two mismatches in the data segment, the parity is are the same and overall we have two mismatches. With more mismatches, we can ignore these cases as they are not crucial cases. The sense amplifier now only have to identify between the 2-mismatch cases and the matched cases. Since the driving capability of the 2-mismatch word is twice as strong as that of the 1-mismatch word, the proposed design greatly improves the search speed and the ratio of the design. Fig. 3 shows the 1-mismatchtransient waveforms of the original and the proposedarchitecture during the search operation. In Section III, we are going to proposed a new sense amplifier that reduces the power consumption of the CAM.

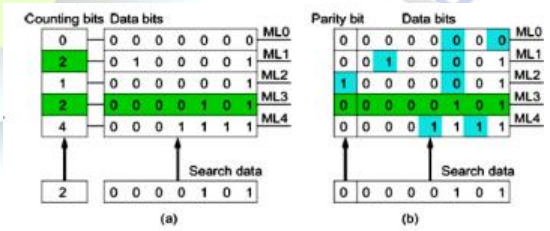


Fig.3. Conceptual view of (a) conventional pre-computation CAM and (b) proposed parity bit based CAM

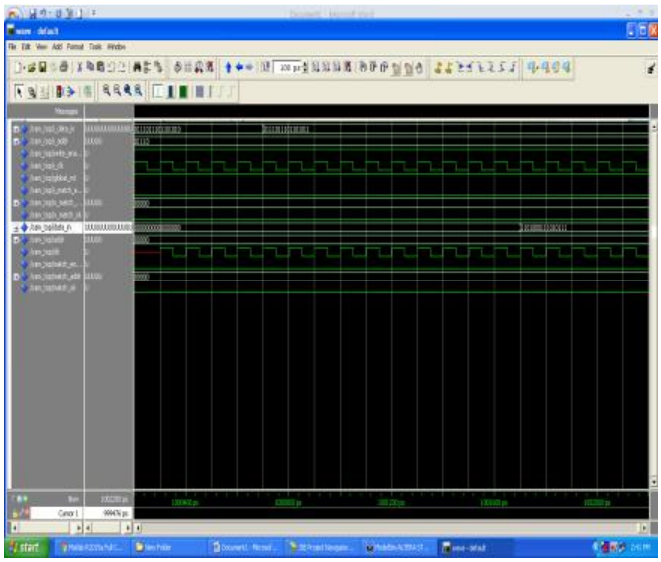
III.SETUP AND RESULT

However, the “COMPARISON” unit, and the “SRAM” unit, i.e.,the cross-coupled inverters, are powered by two separate metal rails respectively. The purpose of having two separate power rails is to completely isolate the SRAM cell from any possibility of power disturbances during COMPARE cycle.As shown in Fig. 4, the gated-power transistor, is controlled by a feedback loop, denoted as “Power Control” which will automatically turn off once the voltage on there aches a certain threshold. At the beginning of each cycle, this first initialized by a global control signal.At this time, signal is set to low and thepower transistor is turned. This will make the signal and initialized to ground and respectively. After that, signal turns *HIGH* and initiates the COMPARE phase. If one or more mismatches happen in the CAM cells, the will be charged up.

the simulation result of the proposed power controller.Section II, the overall search delay is improved by 39%. Thus the new CAM architecture offer both low-power and high-speed operation.

The proposed CAM architecture is TERNARY CAM consists of cells are organized into rows (word) and columns (bit). Each cell has the same number of transistors as the conventional P-type NORCAM and use a similar ML structure. However, the “COM-PARISON” unit, transistors M 1 -M 4 , and the “SRAM” unit.Cross-coupled inverters, are powered by two separate metal rails, namely V DDML and the VDD , respectively. The V DDML is independently controlled by a power transistor (Px) and a feedback loop that can auto turn-off the ML current to save power. The purpose of having two separate power rails of (V DD And V DDML) is to completely isolate the SRAM cell from any possibility of power disturbances during COMPARE cycle.This additional parity bit, in theory, reduces the sensing delay and boosts the driving strength of the 1-mismatch case (which is the worst case) by half.

Binary CAM is the simplest type of CAM which uses data search words consisting entirely of 1s and 0s. **Ternary CAM** (TCAM) allows a third matching state of "X" or "Don't Care" for one or more bits in the stored data word, thus adding flexibility to the search.



OUTPUT

So, you don't need to match the exact address. To match an incoming packet, one needs to match the value & mask pair & compares it with the result

They associate the input compare andwith their memory contents in one clock cycle.They are configurable in multiple formats of widthand depth of search data that allows searches to be

conducted in parallel.CAM can be cascaded to increase the size of lookup tables that they can store.

IV.CONCLUSION AND FUTURE SCOPE

A.Conclusion: In this Paper, architecture of CAM has been reviewed and banked architecture has been proposed. It will get power reduction during comparison, hardware reduction and also over all reduce power dissipation. Hence this method will provide effective usage of power, compare to all other architecture methods because to its parallel match-line comparison, cam is power-hungry. The proposed method Ternary CAM hasbeen used to compare the input data against a table of stored data and returns the address of the matching data.The memory Architecture Z-TCAM that emulates TCAM function with SRAM and has been successfully implemented .

B.Future Scope:

In future Z-TCAM will be implemented to achieve low power and more efficiency. So Z – TCAM will perform independent of data , efficiently handles the wild cards, and has better memory utilization.

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