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POWER AND AREAEFFICIENT ALU DESIGN USING GDI

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***Abstract*—**In the modern era, power dissipation has become a major and vital constraint in electronic industry. Many techniques were already introduced to reduce power dissipation. Gate Diffusion Input (GDI) Technique allows power dissipation to a greater extend compared to the other logic styles. This technique also reduces the transistor count and thus the area of the circuit. Thus the circuit will be much simpler and easy to manage. This paper describes the design of an Eight – bit Arithmetic Logic Unit using Gate Diffusion Input (GDI) Technique and also the comparison with CMOS logic..The arithmetic functions are Addition,Subtraction,Increment, and Decrement operations. The logic functions that can be realized are AND, OR, XOR, and XNOR. The simulation tool used is Tanner EDA45 nm Technology

***Keywords*—VTCMOS, CSLA,GDI,ALU**

I.INTRODUCTION

An Arithmetic and Logic Unit (ALU) is a digital circuit that performs arithmetic and logic operations. The ALU is a fundamental building block of the central processing unit of a computer. The power consumed by the ALU has a direct impact in the power dissipated from the processor. Hence, a design is required to implement the ALU in a fashion where the performance of the processor is improved and also the power consumed is less. To be precise Power consumption of whole data path can be reduced by reducing power consumption of ALU. Adder is the basic building block for an ALU. To reduce the power consumption from ALU first we need to reduce through full adder. Improving the performance of circuits based on CMOS logic by the introduction of many logic styles like Pass Transistor logic, Transmission Gate logic, Double Pass Transistor logic and also many other hybrid logics.Pass Transistor logic is one of the most widely used logics for low power digital circuits. It has many advantages over CMOS, ie high speed, low power dissipation and lower interconnection effects. GDI Technique can overcome certain drawbacks of PTL Logic.

A wide range of complex logic functions in which PTL was used, can be replaced by GDI Technique and this makes the circuit simple. Easier design of fast, low power circuits with less number of transistors are enabled using GDI Technique. Arithmetic and logic operations are the inevitable part of all high speed and low power circuits in the field of microprocessors, digital signal processing and image processing. An Arithmetic Logic Unit with low power dissipation, lesser transistor count and lesser propagation delay can contribute much to the modern era. In this paper an 8-bit ALU is designed using GDI Technique and its power dissipation and transistor count is compared with the CMOS logic. The sub blocks used are multiplexers, adders and gates. The basic logic gates AND, OR, XOR, XNOR and combinational circuits like half adder, full adder, multiplexer etc are designed and compared with the existing logic styles, CMOS and Transmission Gate , in terms of power dissipation and transistor count. Simulation environment is Tanner EDA tool using 45nm technology. The Section 2 previous works.In Section 3, the basic ideas of GDI cell and is operational analysis is discussed. Section 4 deals with the design of basic gates, Carry Select adder and ALU using GDI Technique. In Section 5, simulation results and the discussions are shown. The paper is concluded in Section 6.

II. PREVIOUS WORK

The power consumption of the circuit is mainlydepends on the supply voltage. Reducing the supply voltage will be an effective way to reduce the power consumption. But this in turn reduces the speed of the circuit. Speed also has the prominent role same as the power. In order to achieve same computing speed with reduced supply voltage there is a need to increase the parallelism to compensate for the reduced speed. This increases the complexity of the circuit. Thus there is a trade off in area, power and speed. To reduce the power and to obtain the optimized speed and

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area. The method involves designing a cell in which the logic can be customized by using variable body bias. The cell is made up of VTCMOS transistors in which thebody bias of both PMOS and NMOS is varied based on the logic function. The DTMOS and VTMOS methods provide low leakage compared to CMOS at low voltage but increases the delay and also it is not suitable for cascading stages. In previous methods the transistor count is similar to the conventional CMOS. By varying the body bias in VTCMOS, the leakage can be reduced and the desired logic function can be achieved. The transistor count of the proposed design remains the same irrespective of the logic gates. This reduces the power dissipation as well as the area. The transistor count can be reduced based on the following techniques:

Input Swing

The customizable logic cell is similar to the structure of the inverter that is it consists of one PMOS and NMOS. NAND gate is designed using this techinique,he inputs are given in series so that the input voltages are added and given to the transistors. The above technique is suffers from cascading problem that is even though the input voltages are reduced the output is 5V. This output cannot drive another logic gates designed by this technique. To overcome the above drawback the second technique Resistor network can be chosen.

Resistor Network

In the technique the input swing is maintained at 5V. The structure of the logic cell is maintained. Additionally resistors are used to split the voltages before it reaches the transistor. For each input one resistor is need in addition. Therefore for two input logic gates two resistors are needed in addition. The main drawback of this technique is that it required additional resistor for each input which is equal to a transistor. Thus the area is equal to the conventional static CMOS. To overcome the above drawback the third technique truth table implementation can be used.

Truth Table Implementation

In this technique the inputs are given to all the three terminal of the transistor according to the truth table. This decreases the power and leakage. In NAND gate when the value of input A is logic 0 then irrespective of the input B the output is HIGH. When the value of input A is logic 1 then the output is the invert of the other input B. The logic gates designed using this technique requires minimum number of transistors and hence a considerable power reduction can be achieved. Using this technique half adder and full adder is designed

Carry Select Adder

The CSLA circuit is widely used to alleviate the problem of CPD by independently generating multiple carries and then select a carry to generate the sum. because it uses dual pairs of RCA to generate partial sum and carry by considering carry input C_{in}=0 and C_{in}=1, then the final sum and carry are selected by the multiplexers. Christo Ananth et al. [9] proposed a system in which the complex parallelism technique is used to involve the processing of Substitution Byte, Shift Row, Mix Column and Add Round Key. Using S- Box complex parallelism, the original text is converted into cipher text. From that, we have achieved a 96% energy efficiency in Complex Parallelism Encryption technique and recovering the delay 232 ns. The complex parallelism that merge with parallel mix column and the one task one processor techniques are used. In future, Complex Parallelism single loop technique is used for recovering the original message.

This area size is generally represented as gate count of the circuit. In this way, we can estimate the gate count for entire CSLA circuit

III. PROPOSED WORK

A GDI cell is a new technique for low power circuits In this approach only two transistors are used to implement a wide range of complex logic functions. This technique provides incell swing restoration under certain conditions. GDI Technique can overcome certain drawbacks of CMOS LogicThe basic GDI cell is as shown if Fig. 1. It resembles CMOS inverter in the N: Input to the source or drain of nMOS.

Bulks of both nMOS and pMOS are connected to N or P respectively, so that it can be biased at contrast with a CMOS inverter. The output node: the common diffusion node of both transistors. It can be used as input or output nodes. The basic functions that ca be implemented using GDI cell are shown in the Table.1 first glance. The important difference of the GDI cell from CMOS inverter is that it has three inputs. The three inputs are:

G: The common gate input of nMOS and pMOS.

P: Input to the source or drain of pMOS.

GDI Cell

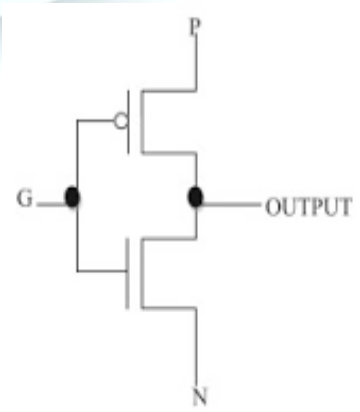

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Figure1. Basic GDI Cell

GDI Cell Functions

Functions are based on the three inputs

N	P	G	OUTPUT	FUNCTION
0	1	A	A'	INVERTER
0	B	A	A'B	F1
B	1	A	A'+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A'B+AC	MUX
B'	B	A	A'B+B'A	XOR
B	B'	A	AB+A'B'	XNOR

Table.1. Basic GDI Cell Functions

IV ALU DESIGN

An ALU is a digital circuit used to perform arithmetic and logic operations. It is the basic building block of the Central Processing Unit (CPU) of a computer. Arithmetic operations like addition, subtraction, increment, decrement, transfer, etc and logic functions like AND, OR, XOR, XNOR etc are performed in ALU. This paper deals with the design of an 8- bit ALU which performs the foresaid functions. The design of ALU is as shown in Fig. 2

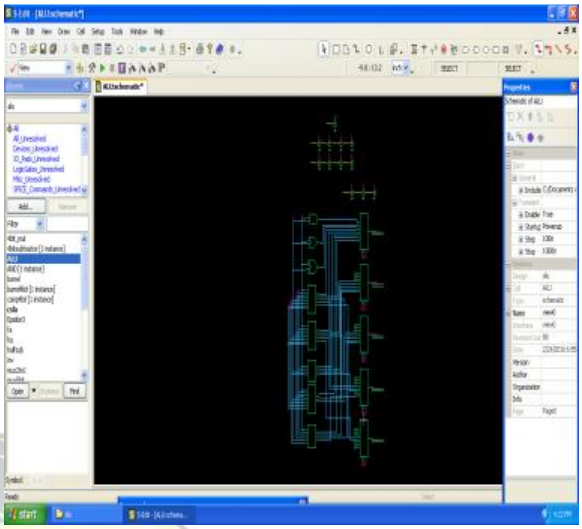

Figure 2. Designof 8- bit ALU

It consists of eight 8x1 multiplexers, full adders, carry select adder, Sutractor,Vedic multiplier,barrel shifter and OR,AND,XOR gates.

ALU Operations

Selection Lines			operations
S0	S1	S2	
0	0	0	AND Gate
0	0	1	OR Gate
0	1	0	EX-OR Gate
0	1	1	CSLA Adder
1	0	0	Sub tractor
1	0	1	Vedic Multiplier
1	1	0	Comparator
1	1	1	Barrel Shifter

Table 2.ALU Operations

Logic Gate Designs

All the Selections lines are low, ALU produce the output for AND ,OR,XOR .AND Gate designs are shown in figure 3,4,5.

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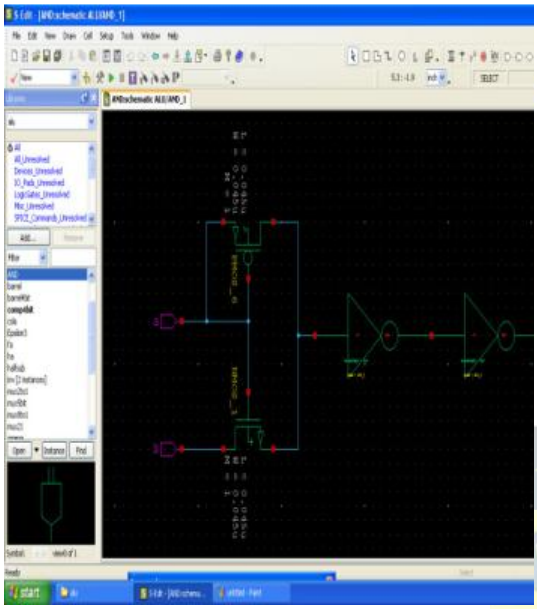

Figure 3.AND Gate Using GDI Cell

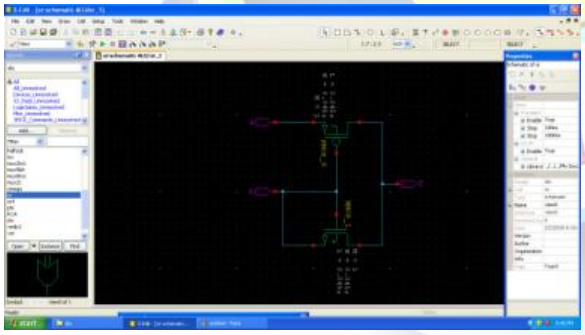

Figure 4.OR Gate Design Using GDI Cell

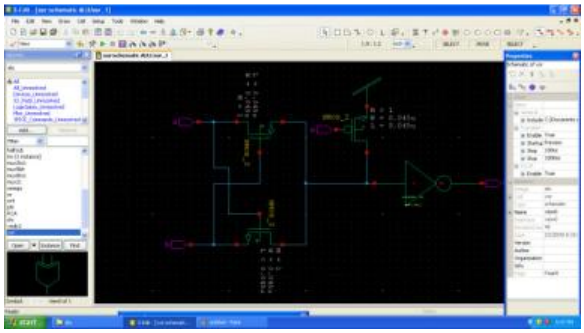

Figure 5.XOR Gate Using GDI Cell

Comparator & Shifter unit

A 4-bit comparator is made with the help of Complementary logic. It compare the two I/Ps and give three states of O/P for three different conditions. Also a 8:1 MUX is made which is used as a cell in the barrel shifter. Used for shifting and rotating operation. Comparator and shifter design is shown in figure 6,7.

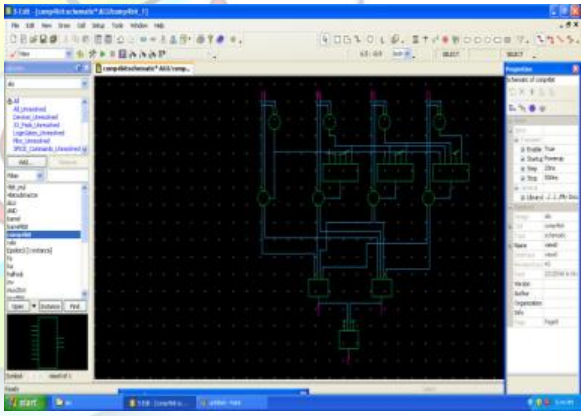

Figure 6.Comparator Design

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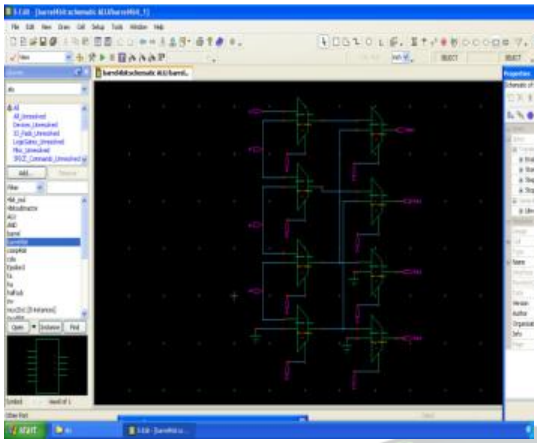

Figure 7.Barrel Shifter design

Vedic Multiplier

Vedic Multiplier is faster than other multiplier like array and Booth multiplier; Area needed is very small compared to other multiplier architecture. Vedic multiplier design is shown in figure 8

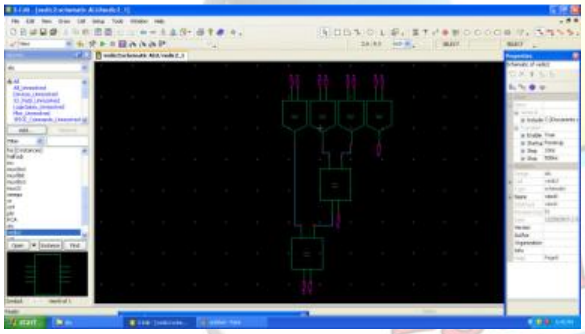

Figure 8 Vedic multiplier design

V. SIMULATION RESULT

The functions are performed on the basis of select line combinations. When S0 = 0, arithmetic functions are performed. Logic functions will be performed when S0 = 1.

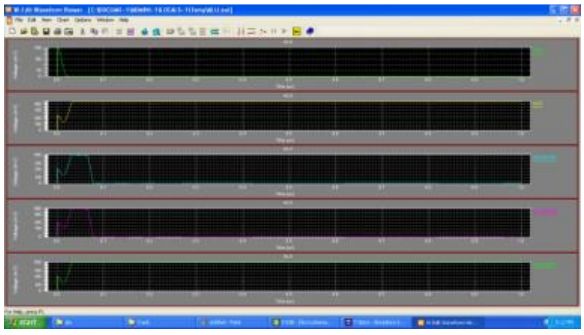

Figure 9.Simulation output of ALU

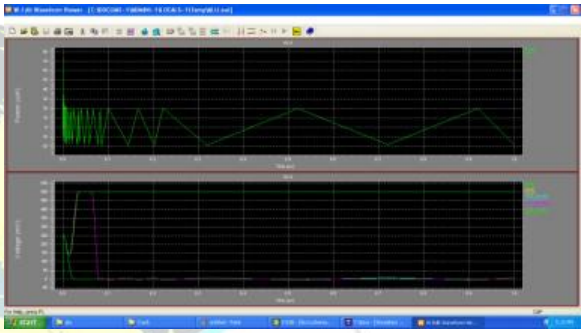

Figure 10.Simulation power of ALU

Utilaization Summary

In our proposed system ,we reduced power and area.so that the circuit complexity level will be reduced.Here the number of transistor can be minimized.The count reduced by using approximate multiplier circuit.

PARAMETERS	EXISTING SYSTEM (CMOS)	PROPOSED SYSTEM (GDI)
Transistor Count	1213	612
Power	9.520402e^-007	1.961853e^-004

Table 3.Comparision Table

VI.CONCLUSION AND FUTURE WORK

This proposed work provides promising result than existing system which concentrates on reduction of power and area thus better performance is achieved than the existing design of ALU. GDI Technique

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reduces the dynamic power dissipation. Since the transistor count is reduced the power dissipation and area of the circuit can be reduced. The proposed work can be extended higer order nanometer applications.

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