ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 3, Special Issue 13, March 2016

# Interleaved Modified SEPIC Converter for Photo Voltaic Applications

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***Abstract*—A design and modelling of Interleaved modified SEPIC Converter with ripple cancellation network is used. The modified SEPIC converter is a high static gain dc-dc converter. The preferred topology presents low switch voltage with high efficiency which can be used for low input and high output voltage appliances. The configuration of this converter is analysed with interleaved concept. The Interleaved modified SEPIC converter has low switching loss,high voltage step up, reduced voltage ripple at the output, faster transient response and reliability. This converter presents a technique for extraction of maximum power from the solar panel. The nature of solar module is non-linear and therefore proper impedance matching is essential to ensure extraction of maximum power. Thus MPPT Algorithm acts as a significant part of solar systems. Here for implementation purpose 21V input voltage and 105V output voltage dc-dc converter operating at 24 kHz switching frequency is constructed. MPPT techniques like Perturb and observe(P&O) and Incremental Conductance(IC) method is used and the comparison is made. The output is implemented and verified by using MATLAB Simulink.**

***Index Terms*— Photo Voltatic(PV), Maximum Power Point Tracking (MPPT) ,Incremental Conductance(IC), Perturb and Observe (P&O), techniques.**

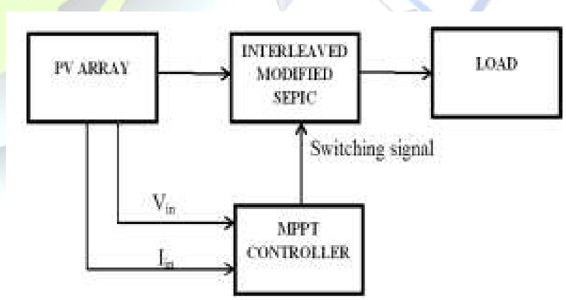
## I. INTRODUCTION

The developing countries like India and China has high energy demand. Unfortunately, due to the increased usage of fossil fuels the conventional power is depleting at high rate. The insufficiency of fossil fuel and increased need for energy has pushed us towards finding alternative sources of energy. There are many different sources of energy such as wind, solar ocean, tidal, thermal, geo-thermal, biomass, nuclear energy etc. Photovoltaic energy is a interesting source of energy; it is renewable, inexhaustible and non-polluting, and it is more and more extensively used as energy sources in various applications. Therefore, solar energy is the important solution for increasing energy crisis.

This solar energy can be transformed into electricity with the aid of solar panel that are made up of silicon photovoltaic cells. The efficiency of solar cells depends on many causes such as temperature, spectral characteristics of sunlight, insolation, shadow, dirt and so on. Changes in insolation on panels due to fast weather changes such as cloudy weather and increase in ambient temperature can lessen the photovoltaic (PV) array output power. In other words, each PV cell generates energy related to its operational and environmental conditions In addressing the poor performance of PV systems, some methods are schemed, among which is a new concept called ―maximum power point tracking‖ (MPPT). All the MPPT algorithm follow the same aim which is maximizing the PV array output power by tracking the maximum power on all operating condition.

The main objective of Interleaved Modifed SEPIC converter is to implement maximum extraction of power from the solar panel under varying conditions using incremental conductance and Perturb and observe method[1]. This converter has reduced voltage ripple at the output, high voltage step up, low switching loss, faster transient response and reliability.

*Proposed Block Diagram*




*Equivalent Circuit*
The equivalent circuit of PV module is given by,

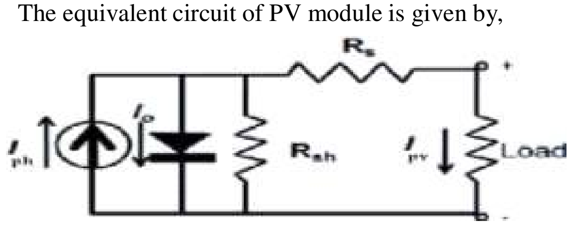



Fig. 1. Block diagram representation

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ISSN 2394-3785 (Online)
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The current source represents the cell photo current. Rsh and Rs are the intrinsic shunt and series resistance of the cell respectively. Usually the value of Rs is very small and that ofRsh is very large.

Equations of PV module is modeled mathematically is given by,

Module photo-current (Iph) ,

**Iph = [Iscr + ki(T − Tr)]X**

Where Iscr is the short circuit current of the PV module at reference temperature, Ki is the short circuit current temperature co-efficient is the module operating temperature, Tr is the reference temperature and X is the module illumination.

Module reverses saturation current- Irs,

**Irs = Iscr/[exp( qVoc / NskAT ) −1]**

Where Voc is the open circuit voltage, q is the electron charge , Ns is the no of cells connected in series , k is the Boltzman constant, A is the ideality factor.

The cell temperature varies with the Module saturation current Io , which is given by **Is=Irs(T/Tr)^3exp((qEg/KA)*(1/Tr-1/T))**

Where Eg is the band gap for silicon.

The current output of pv module is

**Ipv=Iph-Is*[exp{q(Vpv+IpvRs)/NsAKT}-1]**

## II.OPERATION OF PROPOSED CONVERTER

The advantages of interleaved modified SEPIC converter compared to the classical SEPIC converter are low input current ripple, reduced voltage ripple at the output, high efficiency, faster transient response and improved reliability. The below fig.2 represents Interleaved Modified SEPIC converter.

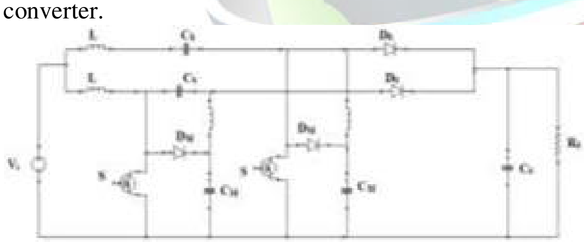

Fig.2.Interleaved Modified SEPIC

In this converter, two Modified SEPIC converter are considered and it is connected in parallel[2]. The two phases of the converter are driven 180 degree out of phase, this is because the phase shift to be given by 360/n where n stands for the number of phases. Since two phases are used the ripple frequency is doubled and outcomes in reduction of voltage ripple at the output side. By this arrangement, the input current ripple is also reduced.

*First Stage ($t_0$-$t_1$):* At the instant $t_0$, switch S is turned-off and the energy stocked in the input inductor L1 is moved to the output through the capacitor CS and output diode Do and also is transferred to the capacitor CM via the diode DM. Therefore, the switch voltage is equal to the capacitor voltage CM. The energy saved in the inductor L2 is transferred to the output through the diode Do. The first operation stage is shown in below fig.3.[3]

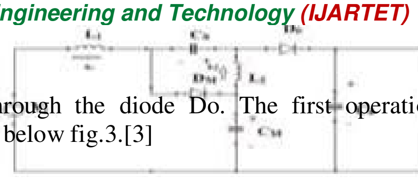

Fig.3.First Stage

*Second Stage ($t_1$-$t_2$ ):* At the instant $t_1$ , switch $S$ is turned-on and the diodes $D_M$ and $D_o$ are obstructed and the inductors $L_1$ and $L_2$ save energy. The input voltage is given to the inductor $L_1$ and the voltage $V_{CS}-V_{CM}$ is given to the inductor $L_2$. The $V_{CM}$ voltage is greater than the $V_{CS}$. The second operation stage is shown in below fig.4

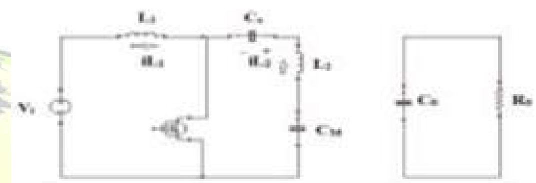

Fig.4.Second Stage

*Main Theoretical Waveform*

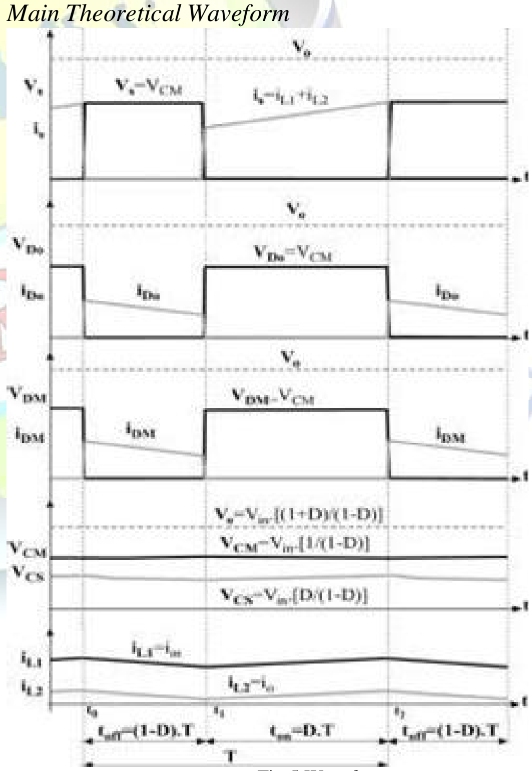

Fig.5.Waveform

*Analysis Of Modified Sepic Converter*

At steady state for the inductor L1,

$V_i (t_{on} + t_{off}) = V_{cm}t_{off}$ (1)

$V_i(DT+(1-D)T)=V_{CM}(1-D)T$ (2)

$V_iT = V_{CM} (1-D)T$

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$V_{CM}$ Capacitor voltage is defined by (3), it is obtained by classical boost converter,

$V_{CM} / V_i = V_i / 1\text{-}D$ (3)

During the period where the power switch is turned off($t_{off}$) the diodes $D_M$ and $D_o$ are in conduction states,

$V_0 = V_{CS} + V_{CM}$ (4)

$V_{CS} = V_0 – V_{CM}$ (5)

The $L_2$ average voltage is zero at steady state, the following relations is considered

$(V_{CM} – V_{CS})T_{on} = (V_0 – V_{CM})T_{off}$ (6)

$(V_{CM} – V_{CS})D = ( V_0 - V_{CM})(1\text{-}D)$ (7)

From equ (3), (5),(6) the static gain of the proposed converter

$(V_{CM}–(V_0 – V_{CM}))T_{on} = ( V_0 – V_{CM})T_{off}$

$2V_{CM}t_{on} + V_{CM}t_{off} = V_0t_{off} + V_0t_{on}$

$V_{CM}(DT+T) = V_0T$

$V_0/V_i = D+1/D\text{-}1$ (8)

The voltage of the series capacitor $V_{CS}$ is defined by substituting (3) & (8) in(7), thus

$V_{CS}/V_i = D/1\text{-}D$ (9)

*Design Considerations*

Output voltage $V_0$=105v, Input voltage=21V, Switching frequency f=24khz,Output power $P_0$ =100W

Switch duty cycle, $D=V_0–V_i/V_0+V_i$ = (105-21)/(105+21)=0.66

Switch and diode voltage,

$V_S=V_{D0}=V_{DM}=V_i/(1\text{-}D)$=21/(1-0.66)=61.76V

$L_1$ and $L_2$ inductance: $L_1 = L_2=V_i*D/\Delta i_L*f$

$L_1 = L_2$ = (21*0.66)/(5*24*10^3)

$L_1 = L_2$ =115μH

Capacitors $C_s$ and $C_m = I_0/\Delta V_c *f$

$I_{D0} = I_{DM} = I_0 = P_0/V_0$ = 100/105 =0.95A

$\Delta V_c = (V_i /(1\text{-}D))*(10/100)$

=(21/(1-0.66)*(10/100)

$\Delta V_c$= 6.176V

$C_s = C_m$ =0.95/(6.176*24*10^3)

$C_s = C_m$ = 6.401μF

Output voltage ripple = (ΔV/V)*100

= [(111.27-111.23)/111.27]*100

= 0.3%

## III MPPT TECHNIQUES

*Perturb And Observe*

In P&O algorithm, small perturbation is introduced in the system. Due to this disturbance, the power of the module changes. If the power enhances due to the perturbation, then the perturbation is carried on in that direction..The power at instant decreases as soon as the maximum power is accomplished. Hence the perturbation reverses[4].

*Flow Chart*

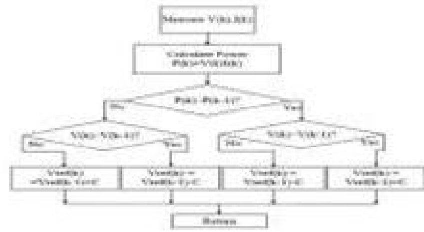

FIG.6.Flow chart of P&O

*Incremental Conductance*

In this method, the array terminal voltage is always altered according to the MPP voltage. It is chosen based on the incremental and instantaneous conductance of the PV module, ie.,at the MPP the slope of the PV array curve is zero as shown in fig.7 represents that increasing on the left of the MPP and reducing on the right-hand side of the MPPT[5] .The equations of incremental conductance are as follows

$di/dv = – i/v$, at MPP (1)

$di/dv > – i/v$ left of MPP (2)

$di/dv < – i/v$ right of MPP (3)

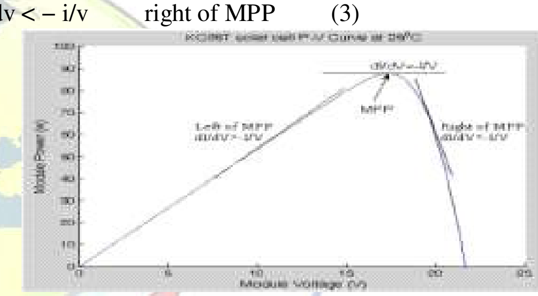


FIG.7. Power Vs Voltage Characteristics

Where, v and i are the PV array output voltage and current respectively. The left-hand side of the equations describes the IC of the PV module, and the right-hand side describes the instantaneous conductance. From (1)–(3), it is evident that when the ratio of the output conductance changes is equal to the negative output conductance, then the solar array will function at the MPP. In other words, by analyzing the conductance at each sampling time, the MPPT tracks the maximum power of the PV module. The accuracy of this method is proven, where it mentions that the IC method can track the accurate MPPs independent of PV array characteristics. The efficiency was observed to be as much as 98.2%, but it is some modifications and reformations were proposed on this method so far, since this method inherently has a good efficiency, the aforestated amendments increase the complexity and cost of the system and there is no remarkable change in system efficiency.

The variable-step-size IC method has been analyzed with the fixed-step-size one. The variable step size with the constant-voltage-tracking startup system has a performance range of 99.2%, while that of the fixed step size has good performance as much as 98.9% due to the chosen small step size. Hence, it is proved that with proper step size selection, the efficiency of the IC method is satisfactory.

## III SIMULATION RESULTS

*(A)Proposed Converter With Pv Module And Mppt (Incremental Conductance)*

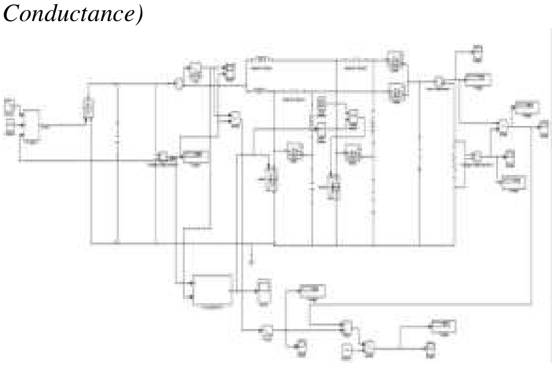

Fig.8 Simulink Model of Proposed converter with IC

*Output Voltage Of Proposed Converter*

The required output voltage and current are obtained as per the design calculations.

For 21V input to the converter, it gives output as 111v.

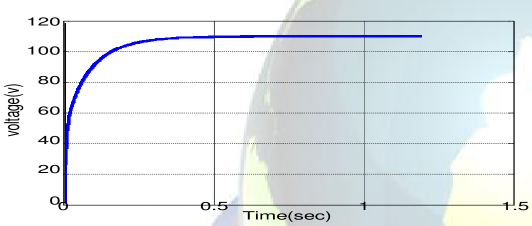


Fig.9 Output Voltage

*Output Current Of The Proposed Converter*

The output current measured for the converter is 1.1 A.

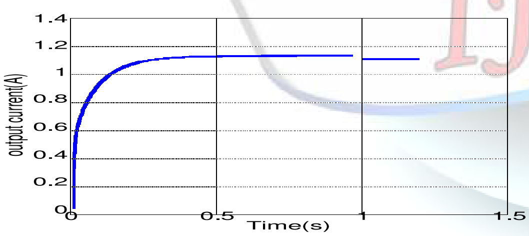


Fig.10 Output current

*Output Power Of The Proposed Converter*

The output power for the converter is 123 Watts.

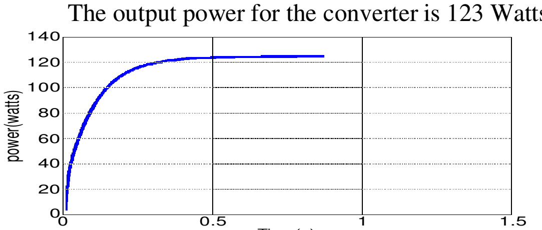


Fig.11 Output Power

*(B)Proposed Converter With Pv Module And Mppt(Perturb And Observe)*

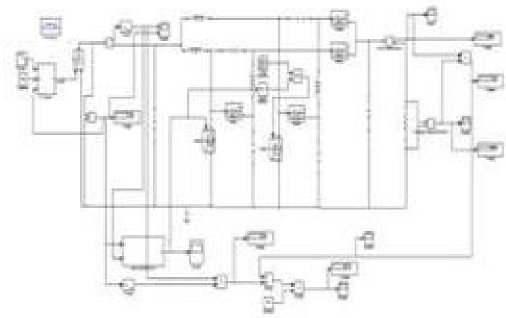

Fig.12 Simulink Model Of Proposed Converter With P&O

*Output Voltage Of Proposed Converter*

As per deisgn calculaitons required output voltlage and current is obtained .

For 21V input to the converter, it gives output as 108.6v.

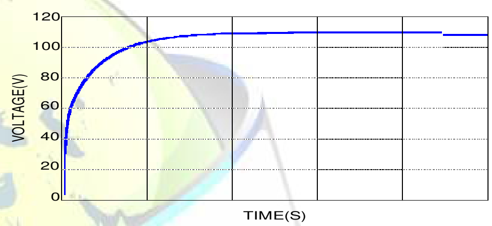


Fig.13 Output voltage

*Output Current Of Proposed Converter*

The output current measured for the converter is 1.086A.

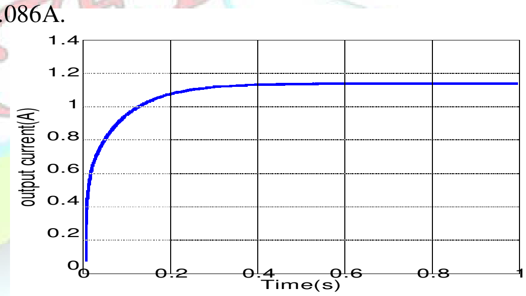


Fig.14 Output current

***Output Power Of Proposed Converter***

The output power for the converter is 118 Watts

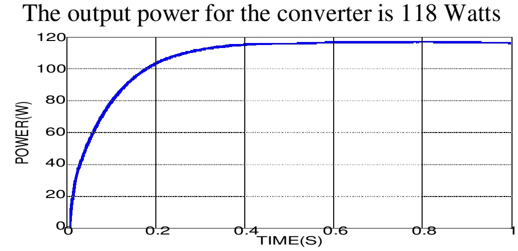


Fig.15 Output Power

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
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International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 3, Special Issue 13, March 2016

*Comparison Between P&O And Incremental Conductance*

| *P&O* | *IO* |
|---|---|
| Output voltage=108.6V | Output Voltage=111V |
| Output current=1.086A | Output current=1.1A |
| Output power=118watts | Output power=123watts |
| Efficiency=85.71% | Efficiency=88.17% |

## IV CONCLUSION

The Interleaved modified SEPIC converter has reduced voltage ripple at the output,high voltage step up, low switching loss, faster transient response and reliability. This converter is analysed with perturb and observe and incremental conductance algorithm. Both methods have certain merits and demertis. Choice is to be made regarding which algorithm to be utilized. If the required algorithm is to be easy and not much effort is given on the reduction of the voltage ripple then P&O is more applicable, But if the algorithm has to give a definite operating point and the voltage fluctuation near the MPP is to be decreased, then the IC method is suitable, but this would make the operation complex and more costly.

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