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Trimodal Register File for Micro Processor Using CMOS Switch

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Abstract: The degradation of CMOS devices over the lifetime can cause the severe threat to the system performance and reliability at deep submicron semiconductor technologies. The negative bias temperature instability (NBTI) is among the most important sources of the aging mechanisms. Applying the traditional guardbanding technique to address the decreased speed of devices is too costly. The register files (RFs) employed for performance enhancement and achieving instruction level parallelism simultaneously. However, RF incurs large power consumption owing to the highly frequent access. Meanwhile, as technology scales, bias temperature instability has become a major reliability concern for RF designers. This paper presents an aging-aware trimodal register file (TM-RF) design to enhance the power efficiency. As instructions pass through the pipeline, TM-RF places the bit-cells in different modes based on the register activity, thereby achieving significant power reduction. To meet design constraints of different applications, we present four schemes to implement the proposed design, providing design flexibility

Keywords: Leakage current, low power, register file, aging mechanism

I. INTRODUCTION

As a fundamental part in modern microprocessors, register file (RF) enhances the performance by shrinking the performance gap between microprocessor and memorysystems, as well as increasing instruction level parallelism through implementing register renaming [1]–[3]. However, with aggressive technology scaling, power efficiency and reliability have become two main challenges to RF designers. First, these microprocessors are capable of fetching, decoding, renaming multiple instructions per clock cycle, and on average every instruction requires three accesses (two reads and one write) to RFs. Such frequent access results in increased power consumption [4]. This situation is further exacerbated in simultaneous multithreading (SMT) processors, where the access frequency is increased by multiple threads. It has been reported that RFs consume 25%–37% of the total power in modern microprocessors [5].

Second, as process variation continues to pose challenge to the reliable operation of RF, bias temperature instability (NBTI/PBTI)-induced aging effect is emerging as another important lifetime reliability issue. The conventional methodology to address the decreased speed of devices due to NBTI is guardbanding. The guardbanding is a technique where the operating frequency is reduced in order to overcome the degradation that may be incurred over the lifetime of the devices. For example, a large guardband of 20% in cycle time is required, given that the circuit speed may be reduced by 20% due to NBTI. The conventional guardbanding technique is too expensive because of the worst-case behavior caused by the uneven utilization of different devices on the chip. Moreover, in future technologies, the guardbanding technique may not be suitable to guarantee performance and reliability requirements for future devices [1].

In general, the aging of devices are proportional to the device stress time and the switching frequency of the internal nodes. Therefore, if a device has a highly biased duty cycle ratio, i.e., logic ‘0’ for the pMOS device, it will have a heavy stress and the aging of the device will be accelerated. Since the register file is holding the current processor context, as well as intermediate computation results, the performance and reliability of the register file are very important for high performance and reliable microprocessor design. However, due to the presence of the narrow-width values (the data with many leading 0s/1s can be represented by fewer bits than the full data width), integer register files suffer a very highly biased duty cycle ratio, thus a heavy NBTI stress, especially for these leading 0s nodes in the register entries. If we adopt the traditional

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guardbanding design based on the worst-case behavior, it will result in dramatic increases in the guardbands and estimated devices failures. Therefore, microarchitecture solutions to balance the utilization and the aging stress areneeded.

II. TRIMODAL REGISTER FILE (TM-RF)

The TM-RF bit-cell provides three different modes: normal work mode, lowleakage data-retention drowsy mode, and minimum-leakage dead mode. The fundamental idea is that, based on the states of a register, the trimodal control logic generates control signals and then passed them to RF, placing the corresponding bitcellsinto the appropriate mode. Specifically, when a register is in ready state, its bit-cells are in work mode to keep valid data effectively; as the register enters the idle state, its bit-cells can be placed in drowsy state for recovery; once the register is released to free state, its bit-cells become dead mode without keeping valid information. The figure 1 shows the proposed design

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Figure 1 Proposed TM-RF bit cells

The circuit implementation and architecture design of proposed system is as follows.

a) TM-RF Bit cells

Each TM-RF bit-cell has three different modes determined by two control signals: DEAD and DROWSY. It is shown in figure 2. The transition diagram is shown in figure 3.

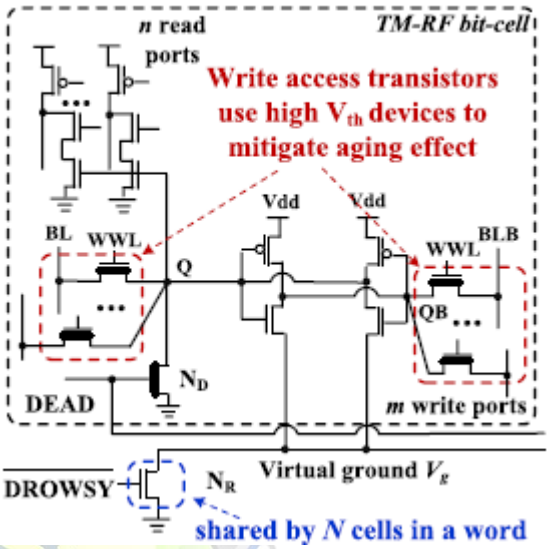

Figure 2 Proposed Trimodal RF bit cells

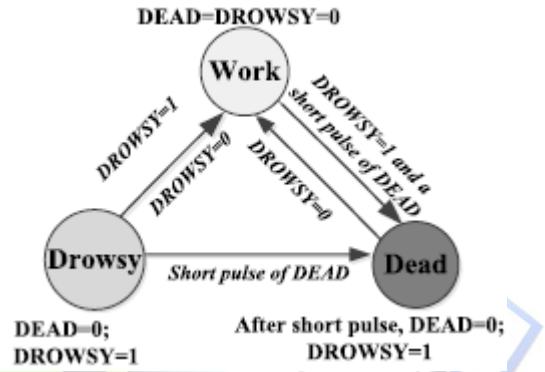

Figure 3 Transaction phase

1) Normal Work Mode (DEAD = DROWSY = 0): In a TM-RF bit-cell shown in Fig. 4(a), if DEAD=DROWSY = 0, the inserted *N*D is maintained cutoff and *N*R is turned on. Therefore, these additional devices do not interfere with normal operations on bit-cells and the working function of TM-RF is similar to a conventional one.

2) Low-Leakage Data-Retention Drowsy Mode (DEAD = 0 and DROWSY = 1): To realize drowsy mode, the gatedground technique [28] is used in our design. While *N*D is turned off, because of the charging leakage current, the node storing 0 goes up and gets saturated quickly. This saturated voltage depends on the size and *V*th of *N*R. By selecting the appropriate size of *N*R, the nMOS transistor which connects the node storing 1 to virtual ground *V*g.

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The dead mode of TM-RF bit-cells provides two additional advantages in terms of power efficiency.

1) When a physical register has been allocated to an architectural register, but before the valid data is written, the register is in empty state and its bit-cells are placed in minimum-leakage dead mode automatically, achieving high power efficiency. From power consumption point of view, TM-RF achieves the same effect as late register allocation technique [11].

2) Similar to the Discharge-RF in [17], because a register with the proposed design stores a 0 by default, writing a 0 to an empty register can be avoided. This can be done by the zero detection as implemented in [17] with negligible hardware overhead.

b) *Aging-Effect-Aware TM-RF Design*

The reliability degradation due to NBTI/PBTI has become a major concern in RF design with the introduction of high-k and metal-gate process (HK + MG) in 32-nm and smaller technologies.

The aging-effect induced *V*th increase influences the performance of SRAM cells including read stability, write margin, access time, and leakage power. As defined HS-SNM is the voltage difference between the disturb voltage on storage nodes and the trip voltage of the inverters (*V*trip*)* in half-select bit-cells during write operations.

III. Architecture Implementation

The architectural mechanisms of the proposed TM-RF are explored in modern microprocessors. The TM control logic is set by the rename logic, as the register renaming logic tracks the state of physical registers. Because most renaming logic is placed close to RF such as Alpha 21 264, the power consumed by the signal transmission from renaming logic to RF can be negligible. Here, we develop two schemes with different implementation complexity.

A. Scheme I-Low Complexity

We first present a simple scheme with minimal hardware support to implement TM-RF [as shown in Figure 4]. In a conventional superscalar microprocessor, the renaming logic has one entry for each physical register to record its status [1]. Typical renaming logic contains Unmap flag, Complete flag, and Counter: Unmap flag indicates whether a register ismapped to an architecture register. Counter is used to record the number of consumers that have not read the information of a register; and complete flag denotes if a register has been redefined [1].

If Unmap = 1, Complete = 1, and Counter = 0, the register can be released. Accordingly, a short DEAD pulse is generated to turn on *NR* and finish discharging process. At the same time, DROWSY is enabled to place the bit-cells to the dead mode.

Once a register is mapped (Unmap = 0), DROWSY = DEAD = 0, TM-RF bit-cells enter the work mode.

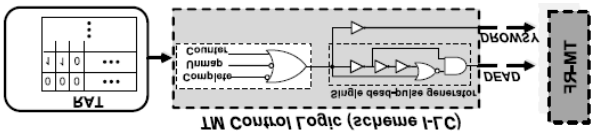

Figure 4 SCHEME I LC

B. Scheme II-High Complexity

This scheme is implemented in conjunction with early register release techniques. As discussed earlier, researchers have explored early register release in two major ways [9], [10]. With hardware support, the first set of solutions release a register when its Redefiner enters the pipeline, instead of waiting for the Redefiner to commit. However, there may be many cycles between a register's LastUser and the dispatch of its Redifiner, missing the opportunity of early releasing. Alternatively, the second set of approaches release registers with compiler support. With compiler analysis, the processor can identify the LastUser and Redefiner of a register, thereby releasing the register earlier. Therefore, we implement TM-RF based on the combination with compiler assist early register technique as shown in figure 5.

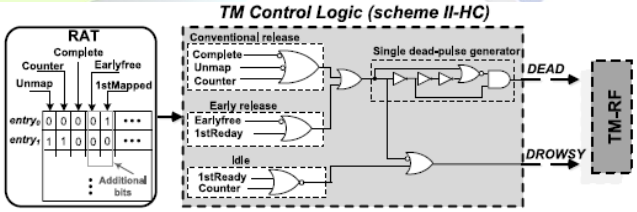

Figure 5 Scheme II HC

IV. Results And Discussion

The RF microprocessor pin design and the power obtained by the RF-MP is shown in figure 6a and 6b For RF Microprocessor.

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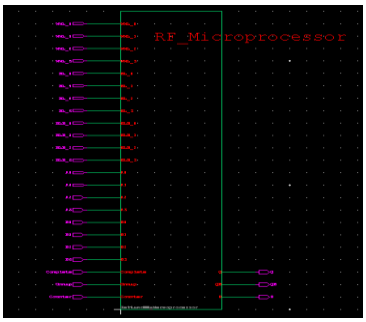

Figure 6 a. Pin Design

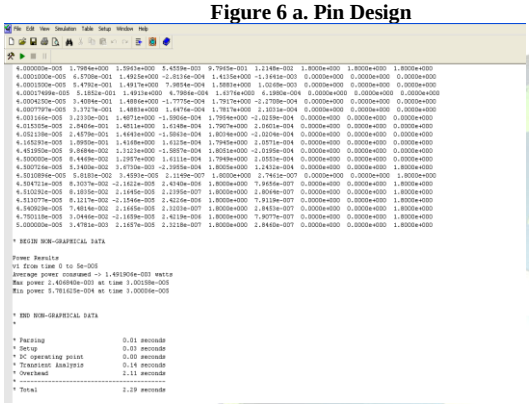

Figure 6 b. Power analysis of RF-MP

The circuit implementation based on schematic design and its waveform output is shown in figure 7a and 7b.

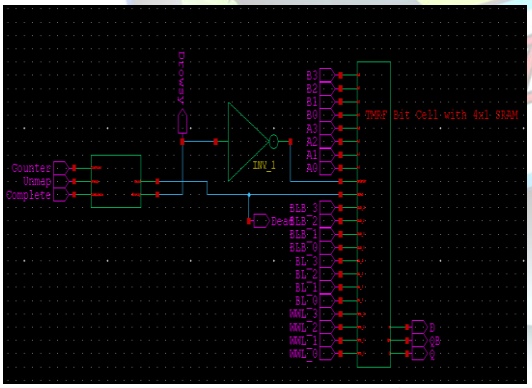

Figure 7 a. Schematic circuit design of RF-MP

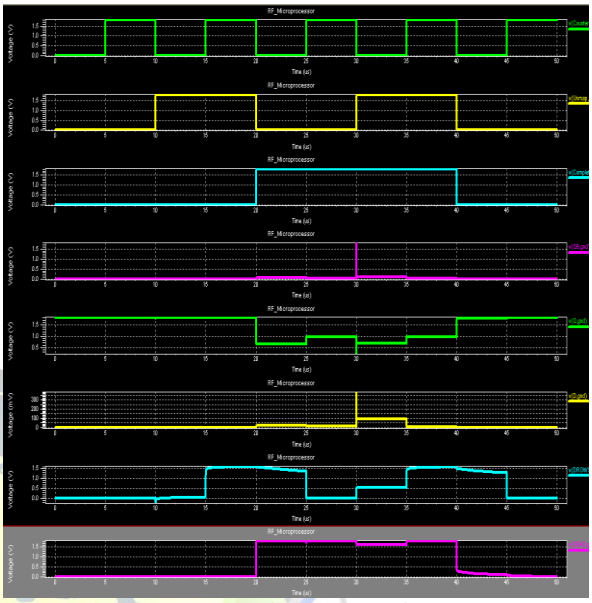

Figure 7 b. Waveform Output of RF-MP

The table 1 shows the following parameters for the conventional RF-MP and Modified RF-MP.

Table 1. Conventional RF-MP vs Modified RF-MP

	Conventional RF-MP	Modified RF-MP
Power consumption	1.068x10¯3	1.491x10¯3
Static power	4.621x10¯3 at time 3.000x10¯5	2.406x10¯3 at time 3.000x10¯5
Static current	2.567x10¯3 A	1.336x10¯3 A
Power Delay Product	13.863x10¯8 W	7.220x10¯8 W
Operating Frequency	100KHz	100KHz
Throughput	200kbps	200kbps

The proposed TMRF based power, schematic circuit and output waveform is shown in figure 8a and 8b and 8c.

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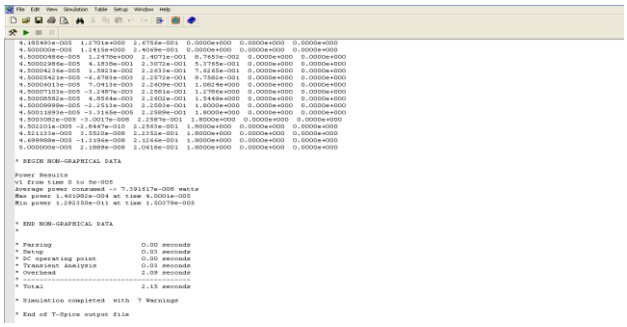

Figure 8a Power Analysis

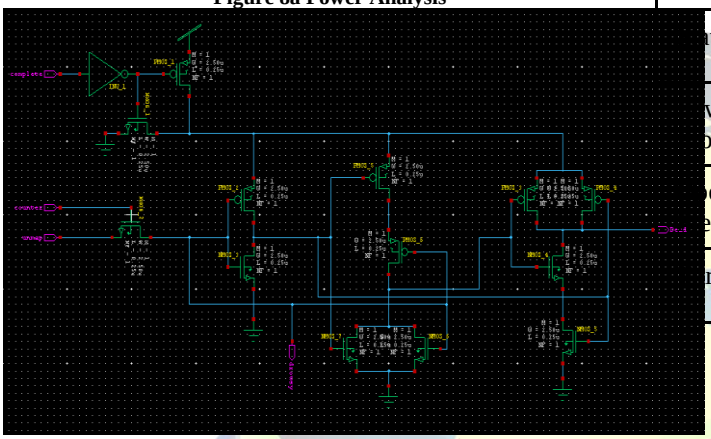

Figure 8b Circuit implementation of TMRF

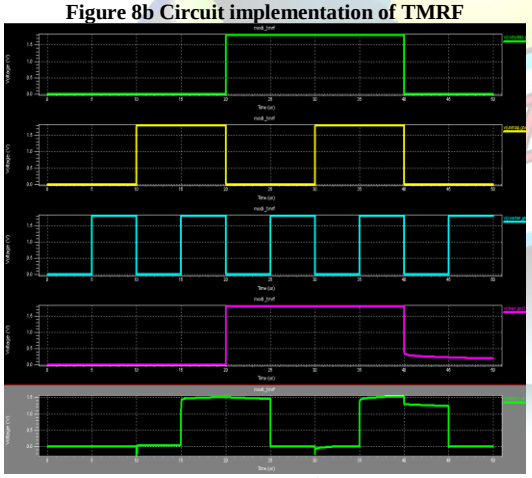

Figure 8c TMRF waveform output

The table 2 shows the following parameters for the conventional TMRF and Modified TMRF.

Table 2. Conventional TMRF vs Modified TMRF

	Conventional TMRF	Modified TMRF
Power consumption	1.376x10¯7	7.391x10¯3
Static power	3.718x10¯3 at time 3.001x10¯5	1.461x10¯3 at time 4.000x10¯5
tic current	2.065x10¯3 A	8.116x10¯5 A
wer Delay oduct	11.15x10¯8 W	5.844x10¯9 W
erating equency	100KHz	100KHz
roughput	200kbps	200kbps

V. Conclusion

In this paper, we have presented a trimodal RF technique for modern microprocessors. The technique employs a trimodal bit-cell and relates these three modes to states of registers, thereby reducing RF power consumption. In existing method no internal memory. We developed four schemes to implement TM-RF, providing flexibility for different applications. We used device selection (high Vth write access devices) and worst case sizing methodology to mitigate aging-effect-induced reliability degradation. Simulation results demonstrate significant reduction in power consumption and noticeable reliability mitigation with minimal area overhead, while maintaining almost the same performance as compared with the conventional design. Our future investigations would include extension of the proposed TM-RF technique to deal with multithreaded workloads.

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