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Transformation of Data in Rise and Fall Time Using DSPWM

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Abstract: PWM techniques to ensure high quality output voltage with reduced harmonics and curved input current irrespective of the load. A double-edged modulation techniques mix each the leading edge and therefore the edge of every pulse move with relation to the unmodulated carrier. The double sampling provides reduced part delay within the management loop over single-edge modulation and solves the massive signal problems associated with the set-reset. The additional benefit of double-edge modulation is that it doubles the rate of the error signal. This paper presents associate 8-/9-bit line-coding scheme to make amends for the temporal arrangement skew between the DPWM and synchronous clock domains whereas limiting the scale of buffering needed within the transmitter and receiver. Moreover, preemphasis is introduced and analyzed as a method to enhance the signal integrity of a DPWM signal. A multiphase-based, time interleaving receiver design employing a sense amplifier is given for high-speed information recovery. The DPWM transceiver is enforced in a 45-nm CMOS semiconducting material on material and operates at 10 Gbit/s with 10−12 bit error rate and consumes 96 mW. the power consumption of the 8-/9-bit secret writing hardware is 1.5 mW at 10 Gbit/s demonstrating low-power overhead.

Keywords: PWM, double edged modulation, line coding, high speed data recovery.

I. INTRODUCTION

The demands of increasing data rate continue to advance the evolution of chip-to-chip interface designs and interconnect architectures. The demands on serial communication have required circuit techniques that optimize spectral efficiency for high data rates [1]–[5]. Channel coding, such as PAM, pulsewidth modulation (PWM) and double-edge PWM (DPWM) have been utilized for memory applications. In Double Edge PWM the Pulse can be Positioned anywhere within the Period. Its called "Double Edge" because both the Edges are Modulated or Varied. In applications like Multi-Phase Motor control Double Edge PWM is used where the Pulse is Center Aligned to reduce Harmonics. For 4-PAM, one symbol consisting of two bits are transmitted during a symbol period.

The symbol period of 4-PAM is twice the bit period of NRZ (2-PAM). Therefore, 4-PAM requires a lower channel bandwidth. However, with a fixed dynamic range, 4-PAM incurs reduced transmitted SNR, compared to NRZ [1]. If the channel response is flat between their Nyquist frequencies, NRZ is recommended because of its simple circuitry. On the contrary, when the channel response demonstrates a sharp frequency roll-off, 4-PAM outperfor ms NRZ. However, previous 4-PAM designs are reported with limitations caused by the reduced dynamic range in the low-supply technology.

According to the transmitted symbols, PWM modulates the pulsewidth on each falling edge. DPWM achieves a doubled bit rate by encoding symbols on both rising and falling edges. These time-domain modulations resolve the limitation of reduced dynamic range. However, time-domain modulations require accurate timing resolution at the receiver. Recent timeto-digital converters of giga-Hz scale with pico-second timing resolution have been verified [7]. Thus, it creates a high potential for multilevel signaling using time domain modulation. In addition, this paper shows DPWM to be as spectrally effective as 4-PAM in terms of the required channel bandwidth. Furthermore, band-limited channels such as multidrop buses can benefit from utilizing DPWM.

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This paper focuses on modulation schemes that require only two signal amplitude levels. As shown in Fig. 1(a), NRZ encodes symbol values in the voltage domain, while the symbol intervals are constant. Fig. 1(b) shows pulsewidth modulation (PWM) encoding of information on the positive pulsewidth, while the interval between rising edges are determined.

The minimum pulsewidth is constrained by the channel bandwidth to avoid significant signal power loss. In Fig. 1(c), multilevel signaling is proposed in the time domain using double-edged PWM (DPWM) to encode information into both positive and negative pulsewidth intervals and has recently been demonstrated to achieve picojoule per bit performance. The advantage of DPWM to NRZ has been presented in a practical channel of multidrop memory link with a channel loss of −32 dB below 5 GHz [8]. At 10 Gbit/s, while NRZ presents a significant eye closure due to the power loss, DPWM concentrates signal power into lower frequencies and, therefore, is less affected to the sharp frequency rolloff.

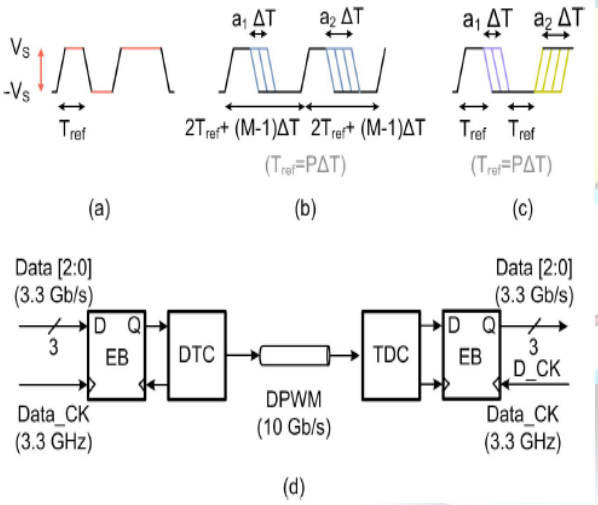

Figure 1 a) NRZ b) PWM c) DPWM and d) DPWM transceiver architecture

II. DPWM SIGNALING

M-ary PWM requires a lower channel bandwidth by encoding multiple bits on the falling edges. Moreover, DPWM presents a doubled bit rate by modulating the signal pulsewidth during both positive and negative excursions as shown in Fig. 2

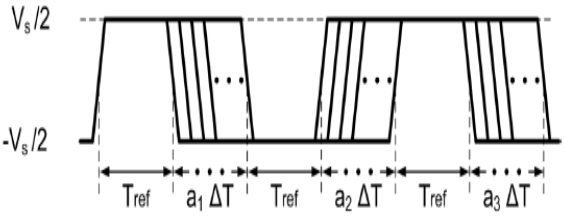

Figure 2 Double-edge M-PWM signaling

DPWM encodes log2*M* information bits representing a symbol *a*[*k*] into both positive and negative pulsewidth, where *M* denotes the total modulation levels. If *a*[*k*] takes a value between 0 to *M* − 1, the period of the DPWM pulsewidth is, $T_{DPWM,\,p/n}[k] = T_{ref} + a[k]\,\Delta T$ Where T_{ref} is the minimum pulsewidth and ΔT is the minimum timing resolution between each symbol. These timing parameters play an important role in defining frequency domain characteristics of the DPWM signaling scheme. The DPWM symbol period is, $T_{DPWM} = E[T_{DPWM,p} + T_{DPWM,n}] = 2\,T_{ref} + (M\text{-}1)\,\Delta T$ Where E is the expectation. Longer *T*ref condenses the signal power to lower frequencies, which can be beneficial in bandwidthlimited channels. *T*ref does not have to be an integer of ΔT, but this assumption simplifies the circuit implementation While *T*ref should be chosen to satisfy the channel bandwidth, _*T* determines the achievable data rate and bit error rate (BER) subject to the accuracy of the time-to-digital conversion. Therefore, the DPWM data rate is calculated from the expected symbol value

$$f_b = \frac{\log_2 M}{E[T_{ref} + a[k]\Delta t]} = \frac{\log_2 M}{T_{ref} + \frac{(M-1)\Delta T}{2}}$$

To adjust the bit rate of DPWM, the number of bits in a symbol is chosen based on the minimum pulsewidth and the timing resolution.

III. DPWM PREEMPHASIS

The preemphasis signals with higher modulation frequencies have lower SNR, so as to compensate this, the high frequency signals are emphasized or boosted in amplitude at the transmitter section of a communication system before the modulation method.That is, the pre emphasis network allows the high frequency modulating signal to modulate the carrier at higher level, this causes more frequency deviation. It is applied to the modulated signal to compensate high-frequency loss in conventional NRZ and PAM signaling. DPWM signaling also improves signal integrity using a feedforward equalizer. The transfer function

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of DPWM signal using an amplitude preemphasis tap weight *G* delayed by a duration *Td* is

$$H(s) = 1 - Ge^{-sTd}$$

Using the first-order Pade approximation, the preemphasis can be modeled as a pole/zero combination where the zero frequency is (1 + G)/(1 − G)(2/Td).

IV. IMPLEMENTATION

Double-edged pulsewidth modulation (DPWM) is less sensitive to frequency-dependent losses in electrical chip-to-chip interconnects. However, the DPWM scheme instantaneously transmits information at a different rate than a synchronous source. The block diagram of the proposed system is shown in figure 2. Furthermore, preemphasis is introduced and analyzed as a means to improve the signal integrity of a DPWM signal. A multiphase-based, time interleaving receiver architecture using a sense amplifier is presented for high-speed data recovery.

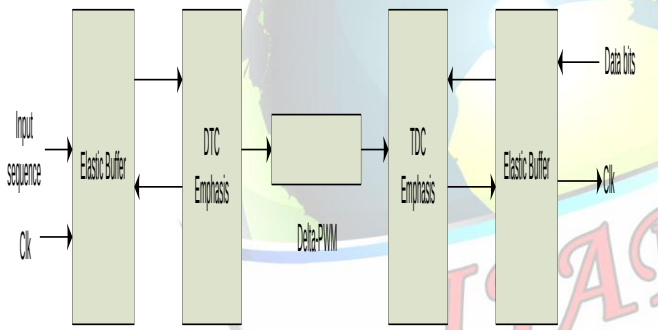

Figure 2 Block Diagram of proposed system

The signal transition time of the DPWM signal is a function of the symbol value as described in. Since data are available from a synchronous data bus, the EB is required to store data until the transmitter is prepared to transmit the data. The EB is a circular shift register with 2*N* BUF word length that can accommodate for the timing skew between the synchronous data clock *ClK* and plesiochronous . In this Method, we are obtaining the data sequence through the concept of Elastic buffer where it is store in the form of Arbiter. DTC and TDC emphasis where performed by means of Integrator and Differentiator formula. In this proposed technique ,we have implemented the delta sigma Pulse width modulation instead of Double edge Pulse width Modulation, Delta-sigma modulation converts the analog voltage into a pulse frequency and is alternatively known as Pulse Density modulation or Pulse Frequency modulation. In general, frequency could vary smoothly in microscopic steps, as may voltage, and each could function an analog of an infinitesimally varied physical variable like acoustic pressure, light intensity, etc. The substitution of frequency for voltage is therefore entirely natural and carries in its train the transmission advantages of a pulse stream.The formula for Delta sigma pulse width modulation is given by,

$$y\,(dsm) = quantize\,(\int (u - y\,(dsm))$$

In which the receive procedure has been implemented by TDC emphasis and Elastic buffer to obtain the correct data sequence.

V. RESULTS AND DISCUSSION

The design utilization for the double edge pulse width modulation is shown in figure 3.

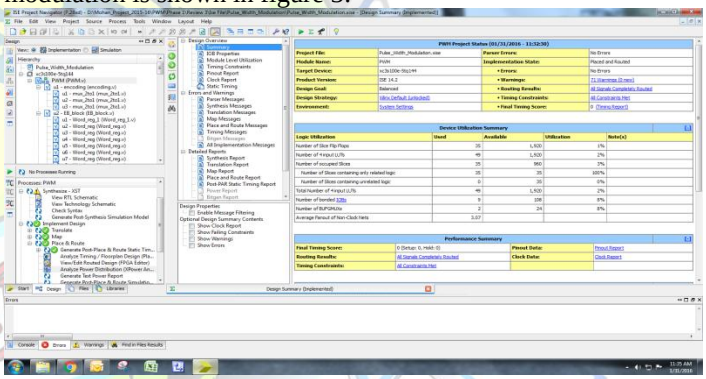

Figure 3 Design Utilization for the double edge PWM

The Delta sigma modulation output using Xilinx software is shown in figure 4.

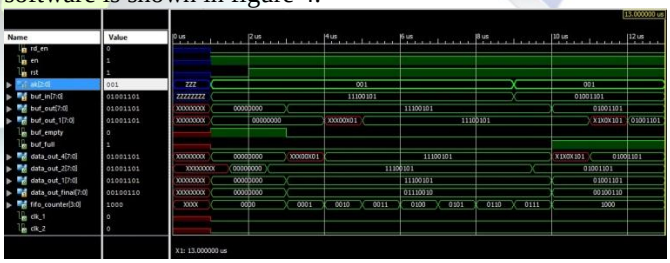

Figure 4 Output of Delta Sigma Serial Communication

The power analyzer for the Delta sigma modulation is shown in figure 5.

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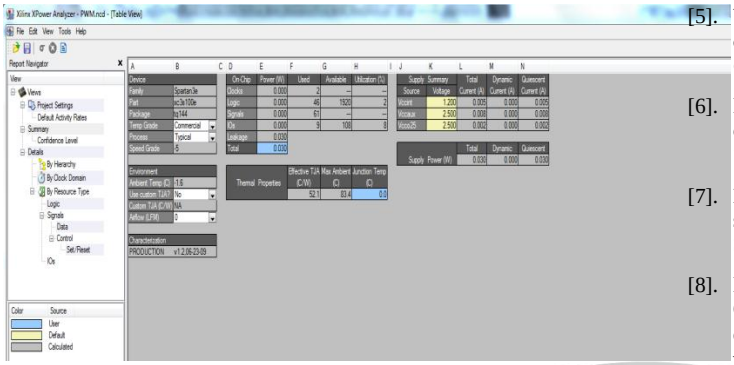

Figure 5 Power Analyzer.

Junction temp: Estimated temperature of the die within the device package is 0^0C.

Total On chip Power: Also referred to as 'Thermal power" (Static design + design Dynamic). Includes power dissipated on-chip from any supply source. Design static is the power when the device is configured and there is no switching activity. Design dynamic is the average power from user logic utilization and switching activity. Here it is around 0.030W

VI. CONCLUSION

This paper presents a high-speed serial I/O scheme based on DPWM. A low-jitter DPWM transceiver architecture is introduced to achieve a finer timing resolution for bit rate enhancement. In future work, we can try to reduce the power by using any adaptive techniques for integrating procedures implemented in the pre emphasis block, thus the power consumption is the major challenge involved in the future work.

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