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VLSI Architecture for Soft SC-FDMA MIMO Detectors Using Linear Block Code

M.Mohanapriyaa[1], Dr.A.Purushothaman[2],
PG Student, VLSI Design,Sree Sakthi Engineering College, Tamilnadu, India[1].
Professor ECE Dept. Sree Sakthi Engineering College, Tamilnadu, India[2].

Abstract: Large-scale multiple-input multiple output is termed to be one of the key technology in future generation multiple cellular systems supporting the 3GPP LTE. LTE includes MIMO technology with orthogonal frequency division-multiple access technology surrounded by the downlink and single carrier-frequency division multiple access (SC-FDMA) within the transmission to attain peak information rates of three hundred Mbps and seventy five Mbps, severally. During this paper a completely unique low-complexity multiple-input multiple-output (MIMO) detector tailored for Single - carrier frequency division-multiple access (SC-FDMA) systems, appropriate for economical hardware implementations. The planned detector starts with AN initial estimate of the transmitted signal supported a minimum mean square error (MMSE) detector. Later on, it acknowledges less reliable symbols that additional candidates within the constellation area unit browsed to boost the initial estimate. An inexpensive highly efficient VLSI design is also introduced achieving advanced performance compared to the standard MMSE detectors. The performance of the planned design is near the prevailing most probability post-detection process (ML-PDP) scheme, whereas leading to a considerably lower complexness.

Keywords: ASIC implementation, LTEm MIMO, SC-FDMA, OFDMA, ML-PDP scheme.

I. INTRODUCTION

Multiple-input multiple-output (MIMO) along with spatial multiplexing [3] develops the basic of most modern wireless communication standards, such as 3GPP LTE [4]–[6] or IEEE 802.11n [7]. MIMO technology avails considerably higher data rates over single-antenna systems by transmitting multiple data streams at the same time as and in the same frequency band. Conventional MIMO wireless systems, though, already start to approach their throughput limits. Consequently, the consumption of new transceiver technologies is of supreme importance in order to meet the ever-growing demand for higher data rates, better link reliability, and improved coverage, without further increasing the communication bandwidth [8]–[10].

The 3rd generation partnership project considered to meet the needs of the 4G wireless communication. LTE along with the multiple-input multiple-output system with \frequency OFDMA technology in the downlink and single carrier-frequency division multiple access (SC-FDMA) in the uplink to accomplish peak data rates of 350 Mbps and 80 Mbps, respectively. LTE-Advanced (LTE- A), which is a progress of LTE, supports single-user spatial multiplexing of up to eight layers in the downlink and four layers in the uplink targeted to achieve peak data rates of 1 Gbps and 500 Mbps, respectively [1].

The SC-FDMA utilizes a discrete Fourier transform-spread OFDM (DFT-S-OFDM) modulation with similar performance compared to the OFDM. Its main advantage is to provide a lower peak-to-average power ratio (PAPR), which makes it the technology of the choice for the uplink [2]. However, the implementation of a MIMO detector in an SC-FDMA system is significantly more complicated than that of an OFDMA system.

This occurs because that sent information is added due to the extra DFT block employed naturally in an SC-FDMA technique. Therefore, the implementation of a low-complexity MIMO detector is needed and is the main challenge in the SC-FDMA framework. Several designs have been proposed for SC-FDMA MIMO detectors among which the linear frequency domain equalizer (FDE) receivers, including the minimum mean square error (MMSE) and zero forcing (ZF), are often used due to their simplicity [2], [5]. Similar to the case of MIMO systems, successive interference cancellation and iterative techniques can be used to enhance the performance of the FDE receivers [11]–[13]. However, these techniques introduce long delays due to their iterative nature.

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The maximum likelihood (ML) receiver also, offers an optimal bit error rate (BER) performance but incurs very high computational complexity particularly in the SC-FDMA receivers. Taking into account the negotiation between the BER performance and the complexity, normally suboptimal methods are engaged. In this paper, a recognition method is suggested for MIMO SC-FDMA systems, which provides near-optimal performance with an important decrease in the complication particularly for huge constellation sizes.

II. MIMO SC-FDMA MODEL

The MIMO single carrier FDMA design model has a transmitter and receiver which are discussed as follows.

a. TRANSMITTER

The transmitter side of a MIMO SC-FDMA system with M_t transmit and M_r receive antennae supporting K users as shown in figure 1.

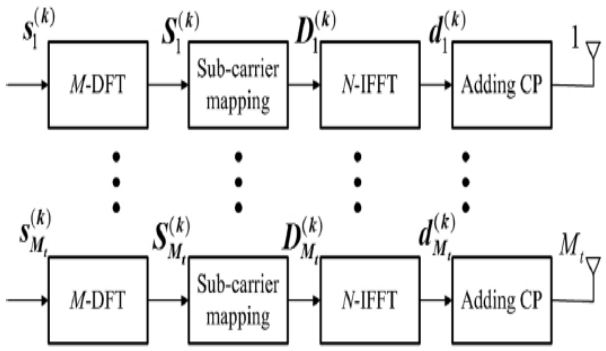

Figure 1 MIMO SC-FDMA Transmitter

The data stream on each transmit antenna is grouped into blocks of M symbols, as follows,

$$\boldsymbol{s_{n_t}^{(k)}} = \left[s_{n_t}^{(k)}(0), s_{n_t}^{(k)}(1), \ldots, s_{n_t}^{(k)}(M-1) \right]^T$$

where the superscript represents the transpose operation, is the antenna index, M is the DFT size.

The next step in the SC-FDMA transmitter is to map the M frequency domain outputs of the FT block to existing orthogonal sub-carriers, denoted by the "Sub-carrier mapping".

b. RECEIVER

A conventional linear SC-FDMA detector for user k is depicted in Figure 2. After the CP removal on antenna n_r at the SC-FDMA receiver with M_r receive antennae, the received signal is denoted as

$$\boldsymbol{r_{n_r}} = \sum_{k=1}^{K} \sum_{n_t=1}^{M_t} h_{n_r,n_t}^{(k)} \otimes_N \boldsymbol{D_{n_t}^{(k)}} + \boldsymbol{w_{n_r}}$$

The transmitted signal of each user can be detected individually, implying that index can be removed.

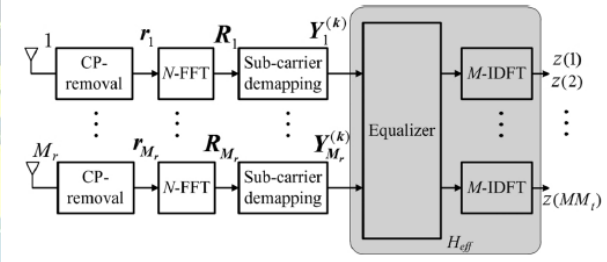

Figure 2 MIMO SC-FDMA receivers

III. PROPOSED SYSTEM

The proposed system architecture is shown in figure 3.

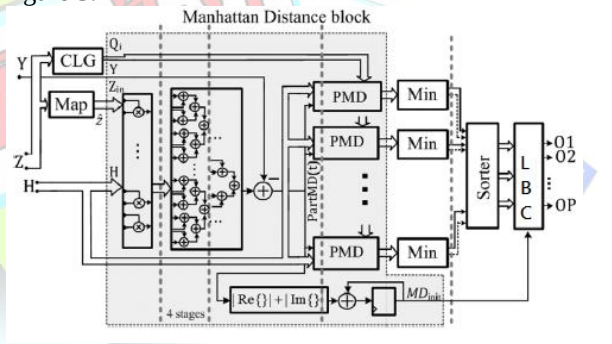

Figure 3 Proposed architecture

The proposed system shown in figure 3 uses LBC (Linear Block Code) to detect and correct the error. Errors corrected in the message block. Encoded using more symbols with accurate original value. The LBC are used in forward error correction and applied in transmitting symbols on a communication channel. The dashed lines in the architecture denote a number of the pipelining stages. The inputs of the architecture are the channel coefficients, the outputs of the MMSE detector, and the received FD signals at the receiver. In fact, the "H" inputs represent the values of all the terms in the t-th row in H_{eff} at the t-th clock cycle, the

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"Z" inputs are the outputs of the first stage, and the "Y" input represents the t-th element in Y at the t-th clock cycle. The architecture performs the detection in clock cycles.

The Min blocks in Fig. 3 calculate the lowest values of the MDs derived by the PMD blocks for each symbol along with their corresponding constellation points. Since P clock cycles are required to produce the EP metric values, the sorting can also be done in P clock cycles using a minimum hardware, which results in the minimum values of the EP metrics and their corresponding constellation points along with indices indicating the symbols selected as the erroneous symbols

IV. RESULT

The design utilization for the SC-FDMA is shown in figure 4.

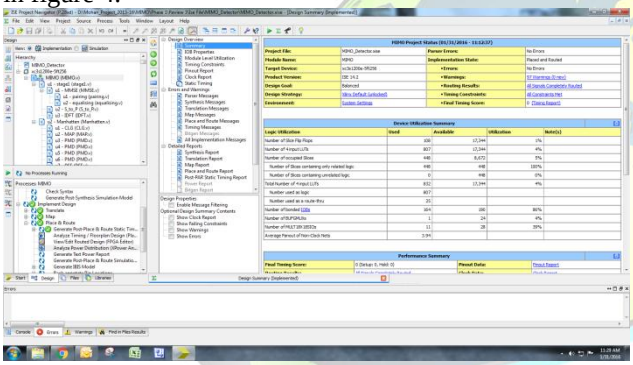

Figure 4 Design Utilization

The power analysis for the SC-FDMA is shown in figure 5. The total power consumed is 0.150Wat the junction temperature of 15°C.

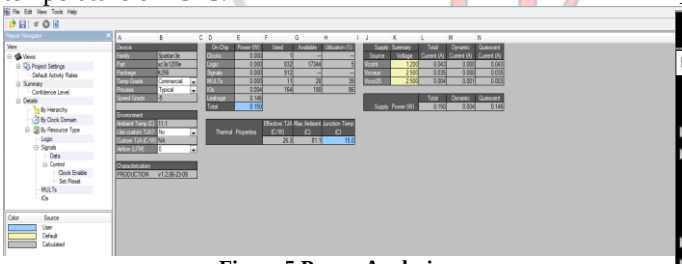

Figure 5 Power Analysis

The figure 6, 7 and 8 shows the MIMO output without acknowledgement and with acknowledgement.

Figure 6 No Output Acknowledgement

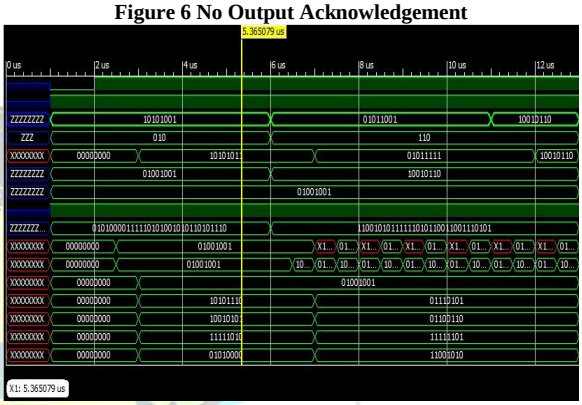

Figure 7 MIMO Output with Acknowledgement

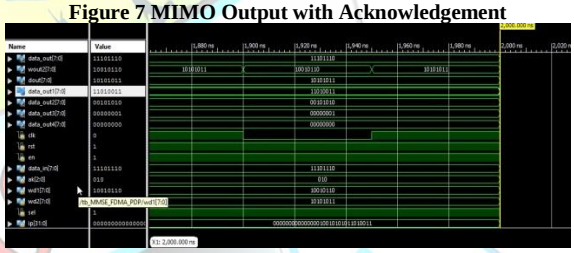

Figure 8 MIMO Output

The LBC output is shown in figure 9.

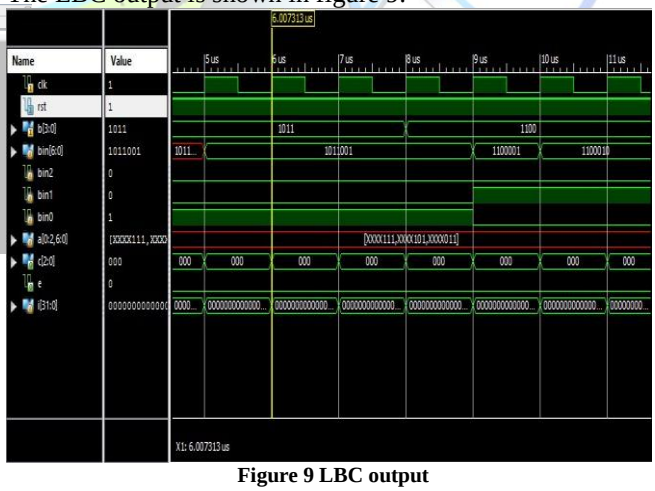

Figure 9 LBC output

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V. CONCLUSION

The architecture of a practical receiver was implemented and tested in an FPGA and ASIC platform for MIMO SC-FDMA systems, resulting in a superior BER performance compared to the MMSE detector and lower complexity compared to current reported designs. The BER performance of the proposed detection scheme is close to ML-PDP while the reduction in the complexity is significant in large constellation sizes. A soft decoding MIMO detector with reasonable complexity was also implemented for a MIMO SC-FDMA coded system, resulting in significant enhancement in the performance. In future, the BER (Bit error Ratio) performance of the proposed detection scheme is close to Previous Methods that has been implemented while the reduction in the complexity is significant in large constellation sizes. A soft decoding MIMO detector with reasonable complexity was also implemented for a MIMO SC-FDMA coded system, resulting in significant enhancement in the performance. By using both the Soft and Hard Decoding methods the given sample BER (Bit error Ratio) could be comparatively reduced and so the complexity of the system.

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Dr.A.Purushothaman received the B.E. degree from the Department of Electronics and Communication Engineering, Anna University, Chennai, Tamil Nadu, India, in 2006, and the M.E. degree in Electronics and Communication Engineering from the Anna University, Chennai, Tamil Nadu, India, in 2008 and the Ph.D.degree from the Department of Information and Communication, Anna University, Chennai, Tamil nadu, India, in 2012. His areas of image and video processing, Signal processing, interest include communication. He has published 10 papers in reputed National / International Journals and more than 6 papers in National/International Conferences. He has obtained a patent on "Compression Artifact reduction and Moving Object Tracking in Image and Video". Coimbatore, Tamil Nadu, India. His current research interests include image processing, video processing, and multimedia systems, and mathematics.

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M.Mohanapriyaa received the B.E degree in Electronics and Communication Engineering from the Tamilnadu college of engineering, Coimbatore in the year 2010. Currently persuing M.E degree specialization in VLSI Design from the Sree Sakthi Engineering College, Coimbatore.