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DESIGN OF VARIABLE LATENCY RELIABLE MULTIPLIER FOR ADAPTIVE FILTERS

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Abstract—*Among the most critical arithmetic functional units Digital multipliers plays the major role. Depends on the throughput of the multiplier the overall performance of these systems can be analysed. By increasing the threshold voltage of the pMOS transistor, and reducing multiplier speed due to the negative bias temperature instability effect occurs when a pMOS transistor is under negative bias (Vgs = −Vdd). A similarly, positive bias temperature instability, occurs when an nMOS transistor is under positive bias. Both properties degrade transistor speed, and the system may fail due to timing violations. Therefore, it is significant to design high-performance reliable multipliers. In the proposed method, we going to design of variable latency reliable multiplier foradaptive filters by identifying the aging of multiplier including the techniques like row bypassing, column bypassing then implementing in the application of adaptive filters using LMS algorithm. In the existing methodology, through the variable latency the multiplier is able to provide higher throughput and the AHL circuit we can moderate performance squalor that is due to the aging effect. Moreover, the proposed architecture can be applied to a column- or row-bypassing multiplier. Experimental result of our proposed architecture of column bypassing or row bypassing reversible logic multipliers can attain higher performance improvement will be compared fixed latency row or column bypassing reversible logic multipliers.*

Keywords—Reversible logic, Adaptive filters, Adaptive hold logic (AHL), Negative bias temperature instability (NBTI), positive bias temperature instability (PBTI)

1. INTRODUCTION

Usersdemand for increasing the portable device yet high performance multimedia and communication products executesstrict constraints on the power consumption of individual internal mechanisms. Multipliers plays the major role in aging aware of the circuits.Due to aging of the circuits the performance of the system degrades and time violations may cause failure of the system. In many applications, such as the Fourier transform, discrete cosine transforms, and digital filtering digital multipliers are among the most critical arithmetic functional units. Negative bias temperature instability (NBTI) occurs when a pMOS transistor is under negative bias and positive bias temperature instability (PBTI), which occurs when an nMOS transistor is under positive bias. It cause interaction of Si and H which breaks Si-H bond by generating H or H_2 molecules. When the biased voltage is detached, the reverse response occurs, dropping the NBTI effect. However, the reverse response does not eliminate all the interface traps generated during the stress phase, and *V*th is increased in the long period.

Hence, it is important to design a high-performance reliable multiplier. The PBTI effect is much smaller when compared with NBTI effect. Aging of the circuit based on these NBTI and PBTI effects. However, this approach can be very doubtful where area and power is inefficient. In traditional circuits the overall clock cycle is achieved correctly by using critical path delay. However, the probability of the critical paths is low. In most cases, the path delay is smaller than the critical pathway. For these noncritical trails, using the critical path delay as the overallcycle period will result in important timing waste. Hence, the variable-latency project was proposed to reduce the timing waste of traditional circuits.

The variable latency design divides the circuit into two types 1). Longer paths 2) shorter paths. Longer paths can execute correctly in two cycle, whereas shorter paths need one cycles to execute. When shorter paths are activated often, variable-latency designs is better than that of traditional designs. In addition, the dangerous trails are divided into two shorter tracks that could be inadequate and the clock sequence is set to the delay of the longer one. These investigation designs were able to reduce the timing waste of traditional circuits to improve performance of the system, but they did not consider the aging effect of the system and could not regulate themselves during the runtime.

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In this proposed method, reversible logic used in multipliers because of its low power consumption. In low power circuit reversible logic is very important. The idea is to build the adder or multiplier circuits using reversible logic. Then implementing this technique in the application of adaptive filters. Adaptive algorithms are a backbone of Digital Signal Processing (DSP). There are many adaptive algorithms but the most commonly used is the Least Mean Square (LMS) algorithm because we can easily vary coefficients to high/low to get desired output.

2. EXISTING METHODOLOGY

2.1 Description

In this existing method we found an aging-aware reliable multiplier design with a novel adaptive hold logic (AHL) circuit. The multiplier is based on the variable-latency technique and can adjust the AHL circuit to achieve reliable operation under the influence of NBTI and PBTI effects. To be specific, the contributions of this paper are summarized as follows,

1) Novel variable-latency multiplier architecture with an AHL circuit. The AHL circuit can choose whether the input patterns need one or two sequences and can alter to ensure that there is least performance squalor after significant aging occurs.
2) Complete analysis and contrast of the multiplier's performance under dissimilar cycle periods to show the usefulness of the existing architecture.
3) An aging-aware reliable multiplier design method that is suitable for great multipliers. Although the experiment is performed in 16- and 32-bit multipliers, existing architecture can be easily extended to large designs.
4) The experimental results show that existing architecture with the 16×16 and 32×32 column-bypassing multipliers can attain up to 62.88% and 76.28% performance improvement compared with the 16 × 16 and 32 × 32 fixed-latency column-bypassing (FLCB) multipliers. In addition, existing architecture with 16 × 16 and 32 × 32 row-bypassing multipliers can achieve up to 80.17% and 69.40% performance improvement as compared with 16×16 and 32×32 fixed-latency row-bypassing multipliers.

2.2. Array Multiplier

The array multiplier is a fast parallel array multiplier. The generation of partial products requires N*M two bit AND gates. Adding of n partial products, which requires N-1, M-bit adders. The shifting of the partial products for their proper alignment's performed by simple routing and does not require any logic

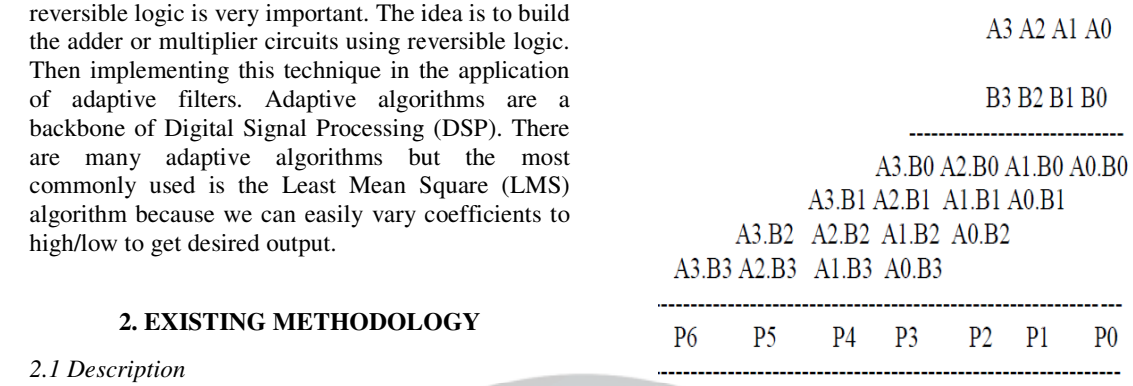

Fig 2.2: 4*4 Array multiplier

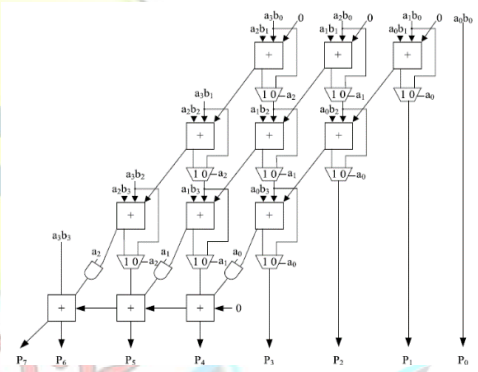

Fig 2.3: Array Multiplier

2.3. Column Bypassing Multiplier

The column-bypassing multiplier is an improvement on the normal array multiplier (AM). Christo Ananth et al. [4] proposed a system in which the complex parallelism technique is used to involve the processing of Substitution Byte, Shift Row, Mix Column and Add Round Key. Using S- Box complex parallelism, the original text is converted into cipher text. From that, we have achieved a 96% energy efficiency in Complex Parallelism Encryption technique and recovering the delay 232 ns. The complex parallelism that merge with parallel mix column and the one task one processor techniques are used. In future, Complex Parallelism single loop technique is used for recovering the original message.

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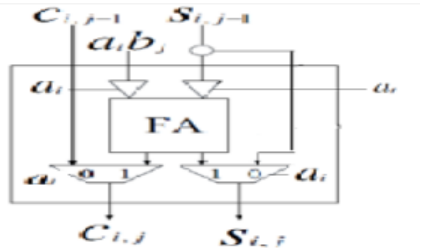

Fig 2.4: Column bypassing adder cell

In 4×4 column-bypassing multiplier. Supposing the inputs are 1010_2 * 1111_2, it can be seen that for the FAs in the first and third diagonals, two of the three input bits are 0: the carry bit from its upper right FA and the partial product *aibi.* Therefore, the output of the adders in both diagonals is 0, and the output sum bit is simply equal to the third bit, which is the sum output of its upper FA. The FA is modified to add two tristate gates and one multiplexer. If *ai* is 0, the inputs of FA are disabled, and the sum bit of the current FA is equal to the sum bit from its upper FA, thus reducing the power consumption of the multiplier. If *ai* is 1, the normal sum result is selected.

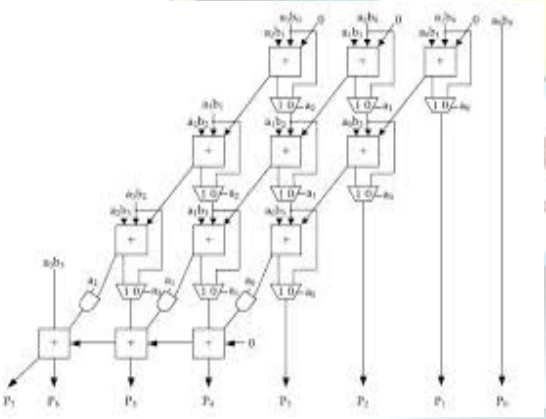

Fig 2.5: Column bypassing Multiplier

2.4. Row Bypassing Multiplier

This method is used to reduce the activity power of the AM. The operation of the low-power row-bypassing multiplier is similar to that of the low-power column-bypassing multiplier, but the selector of the multiplexers and the tristate gates use the multiplicator.

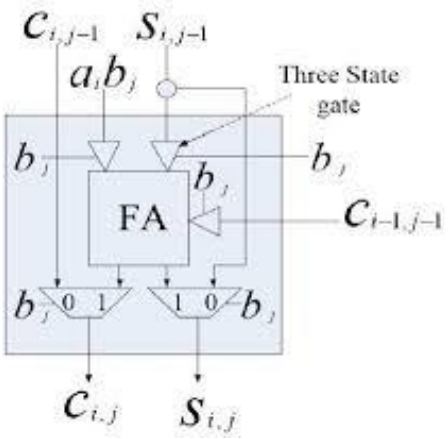

Fig 2.6: Row bypassing adder cell

In 4 × 4 row-bypassing multiplier. Each input is connected to an FA through a tristate gate. When the inputs are 1111_2 * 1001_2, the two inputs in the first and second rows are 0 for FAs. Because *b*1 is 0, the multiplexers in the first row select *aib*0 as the sum bit and select 0 as the carry bit. The inputs are bypassed to FAs in the second rows, and the tristate gates turn off the input paths to the FAs. Therefore, no switching activities occur in the first-row FAs in return, power consumption is reduced. Similarly, because *b*2is 0, no switching activities will occur in the second-row FAs.However, the FAs must be active in the third row because the *b*3 is not zero.

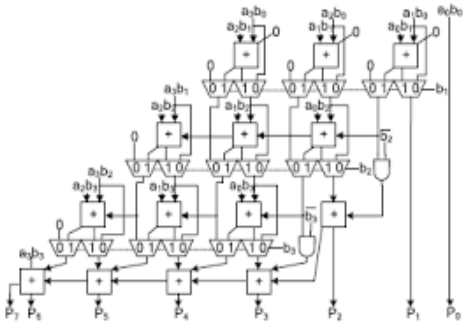

Fig 2.7: Row bypassing Multiplier

3. PROPOSED METHODOLOGY

3.1 Proposed architecture

In this proposed method we found an aging-aware reliable multiplier design with a novel adaptive hold logic (AHL) circuit. The multiplier is based on the variable-latency technique and can adjust the AHL circuit to achieve reliable operation under the influence of NBTI and PBTI effects. To be specific,

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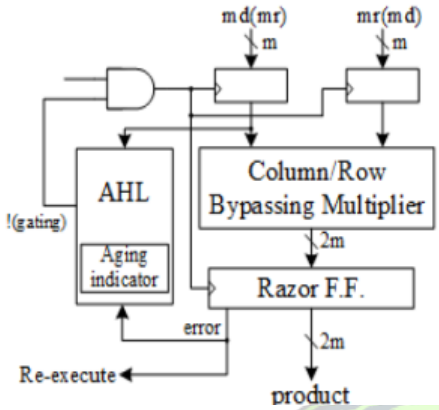

Fig 3.1: Proposed Architecture

Novel variable-latency multiplier architecture with an AHL circuit. The AHL circuit can choose whether the input patterns need one or two sequences and can alter to ensure that there is least performance squalor after significant aging occurs. Complete analysis and difference of the multiplier's performance under dissimilar cycle periods to show the usefulness of the proposed architecture. An aging-aware reliable multiplier design method that is suitable for great multipliers. Although the experiment is performed in 16-bit and 32-bit multipliers, proposed architecture can be easily extended to large designs.Operation of column /row bypassing multiplier is same as the existing methodology. In this method, changing the multipliers design to reversible logic based multipliers. Then applying this techniques in the application of adaptive filters algorithm (LMS Algorithm). Adaptive algorithms are a backbone of Digital Signal Processing (DSP). In order to improve the performance of the reversible multiplier. Experimental result of our proposed architecture of column bypassing or row bypassing reversible logic used multipliers can attain higher performance improvement will be compared fixed latency row or column bypassing reversible logic used multipliers.

4. CONCLUSION

To Design of Variable Latency Reliable Multiplier for Adaptive Filters based on reversible logic.Proposed method is same as that of existing methodology and architecture. The proposed architecture will be applied to a column- or row-bypassing multiplier based on reversible logic multipliers. Then, this method is implemented in the application of adaptive filters algorithm (LMS algorithm). Experimental result of our proposed architecture of column bypassing or row bypassing reversible multipliers able attain higher performance improvement will be compared fixed latency row or column bypassing reversible logic multipliers.

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