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EFFICIENCY OF CONSTANT MULTIPLIER IN RECONFIGURABLE RRC FILTER

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Abstract*—Minimizing the delay and area is a most important in efficient VLSI architecture. The operation of VLSI architecture of interpolation filter for multistandard Digital Up Converter (DUC) by means of two step optimization method is designed, such that area and delay is concentrated. Firstly, the number of multiplication per input sample and number of additions per input sample are reduced when compared to the design of root-raised-cosine Finite Impulse Response filter for multistandard DUC. Multipliers are the basic element of any filter. Hence, a 2-bit (BCS) binary common sub-expression based elimination algorithm has been developed for designing a constant multipliers. This procedure has succeeded in reduced the delay, area and power usage along with 36% improvement in operating frequency compared to the earlier 3-bit BCS-based technique for designing the multistandard DUC.

Index terms — FIR filter, Digital up Converter, Binary Common Sub-expression.

1. INTRODUCTION

1.1 FPGA realization of Modified distributed arithmetic architectures

The design optimization of fully pipelined architectures for area-time-power- efficient implementation of Finite Impulse Response (FIR) filter. The architectures are designed to obtain a suitable area-time tradeoff. Analysis of the performance of different filter orders and different address lengths of partial tables indicate the choice of four input partial tables presents the best of area-time-power-efficient realizations of FIR filter compared with the existing LUT-less DA-based implementations of FIR filters [4] in both high-speed and medium-speed. Hence, by using pipeline register, the choice of 4-bits-per-clock (4BPC) of the architecture for word-length N¼8 with four input partial table yields the best cost-effective when comparing with other different cases in both high-speed and medium-speed implementations.

The major disadvantage is, the proposed technique developed a low efficient DA-based filter.

1.2 Achieving minimum Number of Adders using FIR filter

In this method, the proposed algorithm for the design of low complexity linear phase Finite Impulse Response (FIR) filters with optimum discrete coefficients. This algorithm is based on Mixed Integer Linear Programming (MILP) [1], efficiently traverses the discrete coefficient solutions and searches for the optimum one that results in an implementation using minimum number of adders. During the searching process, discrete coefficients are dynamically synthesized based on a continuously updated sub-expression space.A monitoring mechanism is introduced to enable the algorithm's awareness of optimality. The proposed algorithm can be extended for the optimum design with the maximum adder depth constraint. This method is not convenient for the reduction of hardware and power [1].

1.3 Dynamic Power Consumption by reconfigurable FIR architecture

A low power reconfigurable FIR filter [3] architecture to allow efficient trade-off between the filter performance and computation energy. In the proposed reconfigurable filter, the input data are monitored and the multipliers in the filter are turned off when both the coefficients and inputs are small enough to mitigate the effect on the filter output. Therefore, the proposed reconfigurable filter

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dynamically changes the filter order to achieve significant power savings with minor degradation in performance.According to the mathematical analysis, power savings and filter performance degradation are represented as strong functions of MCSD window size, the input and coefficient thresholds, and input signal characteristics. Numerical results show that the proposed scheme achieves power savings up to 41.9% with less than around 5.34% of area overhead with very graceful degradation in the filter output. The major demerit of this scheme is, it achieves high power savings with less area overhead but it consumes large number of hardware.

1.4 A New Common Sub-expression Elimination Algorithm for Realizing Low-Complexity Higher Order Digital Filter

A new CSE algorithm using binary representation of coefficients for the implementation of higher order FIR filters with a fewer number of adders than CSD-based CSE methods [6]. The CSE method is more efficient in reducing the number of adders needed to realize the multipliers when the filter coefficients are represented in the binary form. From the observation, the number of unpaired bits (i.e.) bits that do not form CSs) is considerably few for binary coefficients compared to CSD coefficients, particularly for higher order FIR filters. The proposed binary-coefficient based CSE method [6] offers good reduction in the number of adders in realizing higher order filters. The reduction of adders is achieved without much increase in critical path length of filter coefficient multipliers. This method is best suited for the implementation of higher order FIR filters but there is no reduction of hardware and power.

1.5 FIR Filters with Low Complexity

Two new reconfigurable architectures of low complexity FIR filters [3], namely, constant shifts method and programmable shifts method. The proposed FIR filter architecture is capable of operating for different word length filter coefficients without any overhead in the hardware circuitry. Dynamically reconfigurable filters can be efficiently implemented by using common sub-expression elimination algorithms. The above architectures has been implemented and tested on Virtex 2v3000ff1152-4 field-programmable gate array and synthesized on 0.18 µm complementary metal–oxide–semiconductor technology with a precision of 16 bits. Design examples show that the proposed architectures offer good area and power reductions and speed improvement compared to the best existing reconfigurable FIR filter implementations. The efficiency is considerably low.

1.6 FIR Algorithm for Implementation in FPGA

A new FIR filter structure that exploits the symmetric coefficients to reduce the hardware in cases where the number of taps is a multiplier of 2 or 3.The proposed algorithm is based on poly-phase decomposition representation and symmetric property of FIR filters. The poly-phase decomposition is for representing the filter in the form of possible number of sub-filters. After the parallel filter being represented in the poly-phase form, then it is represented in the form of traditional FFA [5]. The symmetric property is imposed on those representations which results in half the number of multiplications for a single sub-filter block, which can be reused for the entire tap. Hence, set of symmetric coefficients require only half of the filter length of multiplications for a single filter. High performance and energy efficient implementation also reduce overall power consumption of the system. Time consumed for manufacturing FPGA is high [5].

1.7 FIR implementation Using Wallace Tree Multiplier

Faithfully rounded truncated multipliers with operations of carry save adder by which different parameters are achieved with low cost, high speed and effective results. Direct form of FIR filter utilizes based on Multiple Constant Multiplication Accumulation Truncation (MCMAT) [3] for multiplication and accumulation operations. It will reduce the area by decreasing the number of different components like structural adders and registers. The proposed 12-bit Arithmetic and Logic Unit (ALU) is designed along with Multiple Constant Multiplication Accumulation Truncation (MCMAT) based digital FIR filter for reducing area and increasing speed in real time applications. The advantages of the proposed methods are low cost, high speed and reduced area. However, delay will be noticeable in the output signal.

1.8 Modified Booth Algorithm Based Low Cost FIR Filter Design

A new low area and low cost FIR filter design using a modified Booth multiplier based on direct form

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realization is proposed. Christo Ananth et al. [8] proposed a system which contributes the complex parallelism mechanism to protect the information by using Advanced Encryption Standard (AES) Technique. AES is an encryption algorithm which uses 128 bit as a data and generates a secured data. In Encryption, when cipher key is inserted, the plain text is converted into cipher text by using complex parallelism. Similarly, in decryption, the cipher text is converted into original one by removing a cipher key. The complex parallelism technique involves the process of Substitution Byte, Shift Row, Mix Column and Add Round Key. The above four techniques are used to involve the process of shuffling the message. The complex parallelism is highly secured and the information is not broken by any other intruder.

2. EXISTING METHODOLOGY

2.1 Description of CSM and PSM

To enhance the power consumption, a combination of symmetrical retimed direct form architecture, balanced modular architecture, detached signed processing architecture, and modified (CSD) Canonical Signed Digit technique-based Finite Impulse Response (FIR) filter [5] have been used. Area and power is measured by means of using less number of multipliers for the interpolation. Look Up Tables are used efficiently. An area, delay and power efficient FIR filter [5] by periodical decomposition of Distributed Arithmetic (DA) based on inner-product computation. By using a modified DA technique, high-speed and medium-speed FIR filter architectures are developed. The LUTs are working in parallel for high-speed FIR filter architecture draws a very high current and area consumption.

Common Sub-expression Elimination (CSE) [6] technique, in which multiplication operations are performed by shift and add operations, is known to be most recently used technique. The number of addition operations performs the multiplication operation defines the Logic Depth (LD) of the circuit.

To achieving less hardware footprint with the help of CSE algorithm for implementing higher order digital filters. A low complexity architecture based on Binary CSE (BCSE) algorithm consumes less hardware and power than CSD-CSE method using a common constant/programmable shift-and-add block [6]. Two different types of architecture used for the addition and shift unit,

1. Constant Shift Method (CSM)
2. Programmable Shift Method (PSM)

2.2 Architecture of CSM

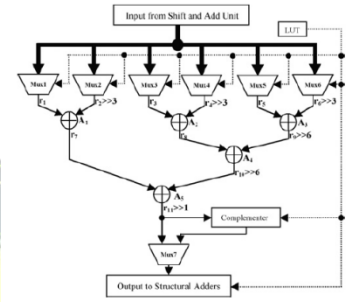

Figure 2.2: Architecture of CSM

2.3 Architecture of Programmable Shift Method

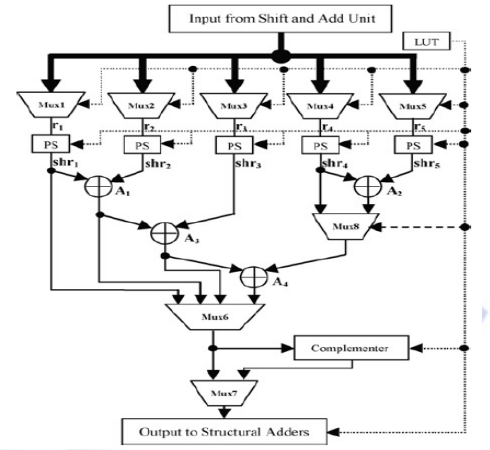

Figure 2.3: Architecture of PSM

3. PROPOSED METHODOLOGY

3.1 Proposed System

A new reconfigurable architecture has been proposed in this project to overcome the discussed disadvantages, for initial reduction of (MPIS) Multiplications Per Input Sample and Additions Per Input Sample (APIS) [1] and subsequent reduction of hardware and power by designing an effectual constant multiplier using 2-bit Binary Common Sub-expression (BCS). Compared with the 3-bit BCS

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based constant multiplier design the 2-bit BCS will leads to achieve good propagation delay.

By comparing all the different algorithm to designing a reconfigurable architecture here 2-bit BCSE is the best method for optimize the area, delay and power. Here dynamic power is considered while designing an efficient architecture. Structure of reconfigurable RRC filter is shown below,

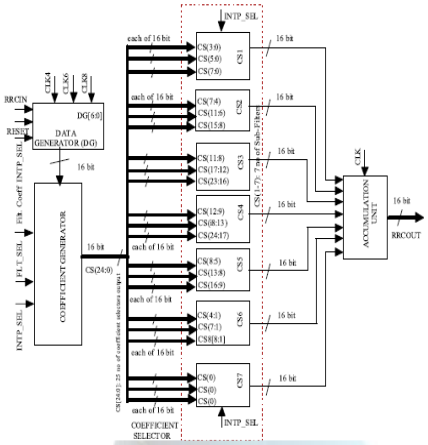

Fig 3.1: Reconfigurable RRC filter

3.2. Coefficient Generator (CG)

The Coefficient Generator unit performs the multiplication between the filter coefficients and the inputs. The proposed two phase optimization method helps to reducing the hardware usage by a substantial amount to facilitate reconfigurable FIR filter [5] implementation with low computation time and low complexity.

The Coefficient Generator block flow diagram for programmable coefficient sets is shown below in figure 4.3. The code generator includes the following blocks namely, (FCP) First Coding pass, (SCP) Second Coding Pass,(PPG) Partial Product Generator, Multiplexer Unit (MU) and Final Addition (FA) block.

The functionality of each block represented in fig 3.2 is described as follows.

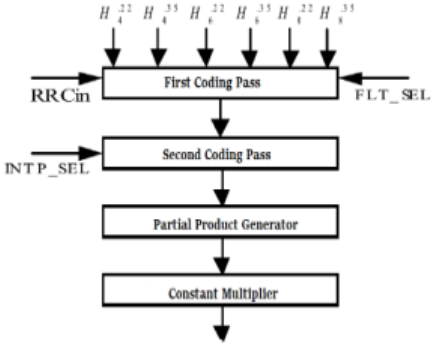

Figure 3.2Coefficient Generator Block

3.3 Constant Multiplier

Constant multiplier architecture is used to minimize the number of addition and multiplication operation by proposing the shifting process. By compare with different multiplier process constant multiplier is the major technique to minimize the MPIS and APIS. The Constant multiplier architecture is shown in fig 3.3

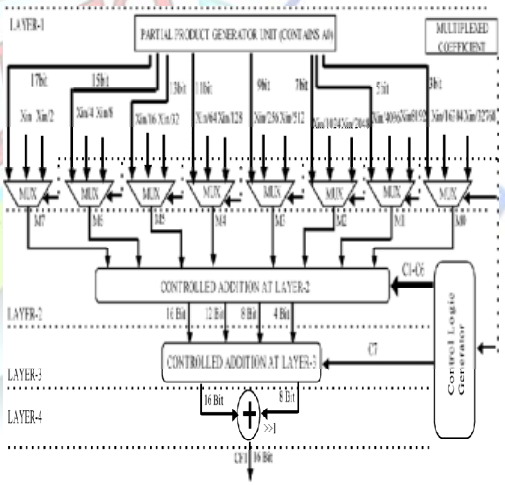

Figure 3.3Constant multiplier Block

4. CONCLUSION AND FUTURE SCOPE

Different problems has been encountered while the reduction of Multiplication Per Input Sample and Reduction Per Input Sample with the

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help of Constant multiplier. If the constant multiplier is processed, the area and delay should be augmented.Binary Common Subexpression Elimination methods are implemented in constant multiplier to reduce the addition and multiplication unit.The number of gates has to be reduced for obtaining the minimum area and delay and shifting operation is performed while considering the constant multiplier is processed.

A constant addition and multiplication less architecture is used instead of using the coefficient selector Unit. Number of addition and multiplication operation should minimized by using the 2-bit BCSE algorithm with the help of multiplexer unit in the aim of optimizing area and delay.

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