EFFICIENT TEST DATA COMPRESSION USING DICTIONARY AND BITMASKING ON FPGA

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Abstract*—We have proposed a capable test data compression using dictionary based coding and bitmasking technique. Enormous test data volume and chip temperature are two major challenges for test engineers. Temperature of a chip can be abridged to a large extent by minimizing transition count in scan chains using competent don't-care filling. The bitstream compression technique to reduce the bitstream size and memory constraint.It also improves communication bandwidth and decreases reconfiguration time. It also for the fast decompression process. Although, both of the troubles rely on don't-care bit filling, most of the existing works have measured them as separate problems. We have combined both temperature decrease and compression into a single problem and solved it. We present antransitional approach that perform a tradeoff between temperature and compression ratio. Practical results on ISCAS'89 and ITC'99 benchmarks show the litheness of the projected method to attain a balance between temperature and compression ratio.

***IndexTerms*—**Compression ratio, temperature reduction, don't-care bits, dictionary based coding,bitmasking,decompression.

I. INTRODUCTION

With increasing intricacy of present day's integrated circuits (IC), the amount of test data needed to test the ICs has increased dramatically. More test patterns are requiredto improve fault coverage targeting delay faults, stuck-at faults and some additional subtle faults. Automatic Test Equipment (ATE) has to contain a large amount of test data, increasing memory size as well as memory cost. Increasing test data volume also results in longer test application time (TAT), which considerably increases total test cost. Built inself- test (BIST) is an another solution which avoids the usage of external storage to store test data. It is moderately costly to employ memory with more capacity and access bandwidth, bitstream compression technique reduce the memory constraint by falling the size of the bitstream. The compressed bit-streams stores more design information using the same memory. However, it suffers from random-resistant faults and bus conflict during test application leading to inadequate fault coverage [1]. The other alternative is test data compression, which stores vast amount of test data (*TD*) in ATE in a compressed form (*TE*), helps to decrease the total memory condition. The compressed data(*TE*) have to pass through a decompressor to get back unique uncompressed (*TD*) test patterns before being applied to the circuit under test (CUT). It is worth mentioning that, more than 95% bits of the test data are don't-cares [2]. To get better compression, most of the test compression techniques take the benefit of the flexibility of don't-care bits, which can be flipped either to '0' or '1' to get more numbers of matching sub vectors from the test vectors without compromising fault coverage. The efficiency of bitstream compression is considered using Compression Ratio (CR). It is define as the ratio between the compressed bitstream size (CS) and the unique bitstream size (OS) (CR=CS/OS). Christo Ananth et al. [5] proposed a system in which the complex parallelism technique is used to involve the processing of Substitution Byte, Shift Row, Mix Column and Add Round Key. Using S- Box complex parallelism, the original text is converted into cipher text. From that, we have achieved a 96% energy efficiency in Complex Parallelism Encryption technique and recovering the delay 232 ns. The complex parallelism that merge with parallel mix column and the one task one processor techniques are used. In future, Complex Parallelism single loop technique is used for recovering the original message. In the literature, these two problems have been solved unconnectedly. Test data compression works try to fill up the don't-care bits to get better compressionratio ignore the thermal effect, while thermal-aware don'tcarefilling works try to reduce temperature by efficientdon't-care bit filling without taking care of test data compression.It may so happen that, for a exacting don't-care bit,better compression can be achieved if it is filled with '0' value,while a '1' value for that bit produces lower temperaturesduring testing. A trade-off between these two don't-care bitfilling techniques is necessary to obtain a good compressionratio with practically low temperature.In recent times, some works have addressed the problem ofhigh power utilization in test data compression schemes. However, it may be noted that, power minimization mayreduce overall temperature of a circuit, but, does not essentiallyminimize peak temperature, which causes local hotspotdue to non-uniform spatial power sharing in the circuitand hence permanent damage of it. The peak temperature ofa block depends not only on power consumption, but also onheat exchange between neighboring blocks. So, the temperatureof a circuit require special attention.In this paper, we have first shown the subsistence of variation in peak temperature of a circuit for a different collection ofdon't-care bit filling targeted towards compression. A thermal aware test data compression technique, which can fill up the don't-care bits smartly taking care of compression and temperature concurrently, has also been presented.This technique efficiently bridge the gap between test data compression and thermal-aware don't-care filling techniques. To the best of our facts, this is the first work, which addresses temperature reduction in test data compression schemes. The respite of the paper is organised as follows. Section II describe the background of a dictionary based coding scheme, which we have used in our work. Motivation of the current work has been offered in Section III. Variation of temperature with a dissimilar clique selection for compression has been shown in Section IV. Section V propose a thermal aware test data compression scheme. Experimental results on different ISCAS'89 and ITC'99 benchmarks have been offered in Section VI. Section VII draw the conclusion.

II. BACKGROUND OF DICTIONARY BASED TEST DATA COMPRESSION

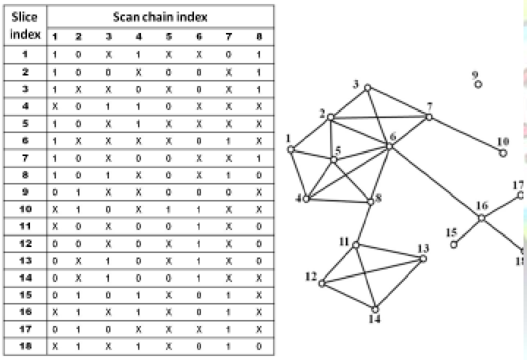
We have used a dictionary based coding technique for compression [1]. It is aadmired test data compression technique in which the total test set is partitioned into several smaller equal-sized test slices. Suppose n test patterns, each of length L arenecessary to test a circuit. Total test data can be considered as $TD = n \times L$. For a circuit with m number of scan chains, m bits of test data have to be transferred concurrently from ATE to the circuit. Each such m bit data is called a test slice. If the length of a scan chain is l, total number of the slice formed is $n \times l$. The scan cells are divided into scan chains in a manner to keep the scan chains as balanced as potential. However, some don't care bits may be necessary to pad to the shorter length test slices to make all of them equal sized. Two slices A and B can be treated as attuned if for any bit position i, either Ai and Bi ($1 \leq i \leq m$, m is the size of the slice) are equal or at least one of them is a don't-care. A delegate slice of the compatible slices may be stored in a dictionary instead of storing all of them. This helps to reduce the memory size essential to store the test data. However, it may be noted that, dictionary size is kept moderately small to reduce hardware overhead. For a dictionary of size D, there presentative slices from D large compatible set of slicesare stored in the dictionary. The rest of the slices are storeduncompressed in the memory. In dictionary-based coding, asingle bit prefix is used to identify whether a slice belongsto the dictionary or not. The slices, whose legislatureare stored in the dictionary, are denoted by a code of length_$log2|D|$_+1, while the code length for the rest of the slicesis $m + 1$. collection of D largest compatible set of slices iscarried out via a clique partitioning heuristic [1]. The slicesare represented by an undirected graph $G = (V,E)$, whereeach slice represent a vertex and the compatibility betweentwo slices is denoted by an edge between them. The cliquepartitioning heuristic tries to find D largest probable cliques from the graph. The representative slices of these cliques arestored in the dictionary. A decompressor is used before CUT toget back the unique patterns from the squashed codewords.

III. MOTIVATION

Any clique partitioning technique uses the give ofdon't-care bits to get the maximum number of matching slices.It may be noted that, most of the don't-care bits present inoriginal patterns get filled up (either 0 or 1) at the time ofgeneration of final patterns after clique partition, where allthe compatible slices belonging to a single clique are replacedby the representative slice corresponding to that clique. Forexample, both of these two compatible slices (10XX01X1)and (X010X1XX) belonging to the same clique, are replacedby the representative slice (101001X1) in the final patterns.An observation from our testing is that around 72%of the total don't-care bits present in original test patternsget filled-up (either 0 or 1) in the clique partitioning process.However, as the clique partitioning is NP-Hard [1], differentheuristics generate dissimilar clique sets. In that case, a slicemay not belong to same clique for different heuristics.The don't-care bits in the final test pattern also change as thedon't-care bits present in a slice may fill up differently if theslice belong to different cliques for different heuristics. It hasa direct impact on the temperature profile of the circuit.The temperature of a circuit largely depends on the activepower consumption, which can be probable from the transitioncounts in the scan cells during shifting of test patternsthrough it. Different test pattern sets cause different thermalprofiles of the circuit. As temperature is a major concernduring testing, it is popular to generate a test pattern setwhich produces a low - temperature profile of the circuit.Test designer has the flexibility to competently fill up the don't carebits present in the original test patterns, to minimize thetemperature of the circuit. Thermal-aware don't-care fillingtechniques fill up the don't-care bits efficiently to minimizetemperature through testing, but may fail to produce a largenumber of compatible slices. This consequences in poor compressionand hence increase the memory size and test cost. It is ademanding issue to fill up the don't-care bits efficiently to producelow temperature during testing, as well as a logicallygood compression ratio. This hasaggravated us to develop a thermal-aware test data compressiontechnique that brings balance between compression ratio andtemperature of the IC.

IV. VARIATION OF TEMPERATURE AND COMPRESSIONRATIO FOR DIFFERENT CLIQUE PARTITIONS

The clique partitioning heuristic presented in [1] startswith the apex with maximum number of neighbours andretrieves the largest clique related with it from the graphand proceeds with searching for the next vertex with maximum neighbors from the remaining members of the graph until allthe vertices have been retrieved.



Slice index	Scan chain index							
	1	2	3	4	5	6	7	8
1	1	0	X	1	X	X	0	1
2	1	0	0	X	0	0	X	1
3	1	X	X	0	X	0	X	1
4	X	0	1	1	0	X	X	X
5	1	0	X	1	X	X	X	X
6	1	X	X	X	X	0	1	X
7	1	0	X	0	0	X	X	1
8	1	0	1	X	0	X	1	0
9	0	1	X	X	0	0	0	X
10	X	1	0	X	1	1	X	X
11	X	0	X	0	0	1	X	0
12	0	0	X	0	X	1	X	0
13	0	X	1	0	X	1	X	0
14	0	X	1	0	0	1	X	X
15	0	1	0	1	X	0	1	X
16	X	1	X	1	X	0	1	X
17	0	1	0	X	X	X	1	X
18	X	1	X	1	X	0	1	0

Figure 1.An example of test data for multiple scan chain set-up and corresponding compatibility graph.

Figure 1. An example of test data for multiple scan chain set-up and matching compatibility graph of starting with vertex with highest neighbours, if we start with every vertex and then explore the total graph to find best possible clique sets from the graph, we get $n\times\ l$ number of clique sets for $n\ \times\ l$ number of vertices. Figure 1 shows an example set of test data distribution in 8 scan chains and resultant compatibility graph of the test data. There is a total of 18 slice, each of which has 8 bits. For this particular example, we can have maximum 18 different clique set. *Clique List CLi* $(1 \leq i \leq (n \times l))$ is a database that stores information concerning all generated cliques from the graph considering *i* as *start vertex*. Some of the don't-care bits of the slices belonging to thesame clique are filled up (either '0' or '1') to form a commonrepresentative slice for all of them.All the slices from a particular clique are replaced by the resultant representative slice of that clique. The customized details of all of the slices are stored in *Slice Info SIi* $(1 \leq i \leq (n\times l))$. These *Slice Info* are used to generate modified test patterns (*TPi*) $(1 \leq i \leq (n\times l))$ corresponding to *CLi*. In the above mention example, the cliques of clique list *CL*1 are *{*1, 2, 5*}*, *{*3, 6, 7*}*, *{*11, 12, 13, 14*}*, *{*4, 8*}*, *{*15, 16*}*, *{*10*}*, *{*17*}*, *{*18*}*, *{*9*}*, while the clique of clique list *CL*2 are *{*2, 3, 6, 7*}*, *{*1, 4, 5*}*, *{*11, 12, 13, 14*}*, *{*15, 16*} {*8*}*, *{*10*}*, *{*17*}*, *{*18*}*, *{*9*}*. It may be noted that, vertex 2 belongs to two different cliques for two different clique partitions. The don't-care bits present in slice 2 also fill up differently for two different belongings. Original slice detail of slice 2 is (100X00X1), which is adapted as (10010001) in *SI*1, while the same slice is modified as (10000011) in *SI*2. Final test pattern sets *TP*1 and *TP*2 also differ from each other. These two different test pattern sets may illustrate different thermal behaviour. We have shown a variation of the thermal profile for different clique selections for several ISCAS'89 and ITC'99 benchmarks. Circuit information regarding the test data volume and number of clique sets generate for different number of scan chains (*NSC*) has been mentioned. Mintest [4] test sets for stuck-at fault are used for ISCAS'89 benchmarks, while test sets for stuck-at fault, generated from TetraMax ATPG tool are used for ITC'99 benchmarks.It shows the difference of peak temperature and compression ratio (CR) for different clique selections. Thermal profile of a circuit has been considered using the thermal simulation steps mentioned below.

- Each Circuit description in Verilog format (.v) has been taken as input and mapped to Faraday 90nm standard cell library. The circuits have been synthesized using Synopsys Design Vision Compiler to generate a gatelevel netlist from the Verilog design explanation.

- All the flip-flops have been replaced by scan flip-flopsusing Synopsys DFT Compiler for the testability idea.Multiple scan chains have also been inserted.
- Encounter RTL-to-GDSII system from pulse [6] hasbeen used to generate floorplan of the given scan insertedpropose using standard cell library.
- The scan inserted netlist and the test patterns have beenfed to a power estimator tool [3]. Power consumption ofeach of the logic elements (gate, flip-flop) with dissimilartypes and inputs has been estimated using SynopsysDesign Vision tool and stored in a database. This databasehas been used to convert the transitions in individuallogic elements into their resultant power valuesduring circuit simulation for each scan shift and captureoperation.
- The floorplan obtain from Cadence Encounter tool [6]has been divided into a number of blocks of same size forthermal simulation. The power trace has been computedfor each of these blocks.
- Thermal simulations have been approved out using thermalsimulation tool HotSpot taking power trace andblock-level floorplan as input.However, accessibility of the power estimator tool [3] hasbeen upgrade from single scan chain operation to multiplescan chain operation.From , a significant variation in peak temperaturecan be notice for different clique selections while the correspondingvariation of CR is reasonably very less. This showthe scope of obtaining good test data compression with lowtemperature profile, by efficient don't-care filling.

A.Bitmask Selection

Bitmask is a pattern of binary values which is combined with some value using bitwise AND with the results that bits in the value in positions where the mask is zero are also set to zero. A bitmask may also be used to set certain bits using bitwise OR, or to invert them using bitwise exclusive or. This move toward tries to include maximum bit changes using mask patterns without adding important cost (extra bits) such that the CR is improved. The compression technique also ensure that the decompression efficiency remains the same compared to that of the existing techniques. belowrepresent compression using bitmask selection. The bit-streams which cannot be compressed use dictionary selection are compressed by bitmask selection. The selection of bitmask plays ansignificant role in bitmask-based compression.

B. Dictionary Selection

Dictionary-based code-compression techniques present compression efficiency as well as fast decompression device. The basic idea is to take commonly happening instruction sequences by using a dictionary. The repeating occurrence are replaced with a code word that points to the guide of the dictionary that contains the pattern. The compressed program consists of both code words and uncompressed information. The binary consists of ten 8-b patterns, i.e.., a total of 80-b. The dictionary has two 8-b entry. The compressed bit-streams requires 62 b, and the dictionary requires 16 b. In this case, the CR is 97.54%. The bit-stream CR for dictionary selection is large therefore it does not yield a superior compression technique. The bit-streams which cannot be compressed using dictionary selection can be compressed by bitmask selection which yield a smaller compression ratio.

V. THERMAL-AWARE COMPRESSION

In the previous section, we have seen the variation in peak temperature and compression ratio with dissimilar clique selections. Although, selecting a solution with lower peak temperature and good compression ratio from all clique lists may be a choice to address both low temperature and good compression issues, however, this method relies on detailed information to find clique set with low temperature and hence may not be applicable for the complex circuits with huge amount of test data. Besides, this method does not fill the don’t-care bits to minimize peak temperature. To get aimportant reduction in the peak temperature of the chip, some thermal-aware don’t-care filling technique has to beincorporated in the clique partitioning heuristic. However,compression ratio may have to be compromised to some degreeto get a good thermal-aware test pattern set.High power consumption during changing of test vectors inthe scan chains plays a main role in temperature increaseof the circuit. Large number of intermediate patterns aregenerate during shifting in (out) of a particular test vectorthrough the scan chains. Power consumption increases becauseof these intermediate pattern.Minimizing the transition count in scan chains by efficientthermal-aware don’t-care filling is a possible solution to reducepeak temperature, as well as circuit power.Thermal-aware don’t-care filling technique presented in[3] produces sensibly low temperature test pattern set. In[3], the entire circuit has been divided into several blocksconsisting of some gates and flip-flops. A power estimationtool [3] identify the flip-flops with high transitions in eachblock. These flip-flops are called critical flip-flops as they playaimportant role in high power consumption of the block. Eachblock has been given a weight as per the power utilization ofthe block. However, as the power of adjacent blocks mayhave a large impact on the temperature of a block,floorplan information of the circuit has to be incorporatedwith the power estimation tool to estimate the temperature ofthe blocks. The temperature of the hottest block with highestpredictable temperature has been tried to minimize with an aimto minimize the peak temperature of the circuit.In this section, we here a *Thermal-Aware CliquePartitioning Heuristic* which can take care of both compressionas well as the temperature of the chip.We have usedthe test pattern set generated using the method describe in[3] as the base case of thermal-aware solution. The don’tcarefilling technique mentioned in [3] can only hold thecircuits with single scan chain set-up. Our adapted thermalawaredon’t-care bit filling technique can fill up don’t-care bitstaking care of the multiple scan chains.

Algorithm 1:*Thermal-Aware Clique Partition Heuristic*input :unique test patterns *TPO* with don’t-care bitsoutput: concluding test patterns *TPFINAL* with a trade-offbetween temperature and compression ratio.

1 Begin.

2 Fill up don’t-care bits presented in the test patternsusing thermal-aware don’t-care bit filling technique[3] to get thermal-aware test patterns *TPTH*;

3 Store the thermal-aware test slices obtain from*TPTH* in thermal-aware *Slice Info* (*SITH*);4 Apply clique partitioning heuristic [1] on *TPO*; Getmatching compression-aware *Clique List*(*CLCM*) and *Slice Info* (*SICM*); Computecompression-aware test pattern *TPCM* from *SICM*;

5 Sort the compression-aware *Clique List* (*CLCM*) indescending order on the basis of the number ofelements present in a clique;

6 Select a weightage factor *Wt* within a range of 0 to1. (0 → thermal-aware don’t-care filling;1→compression-aware don’t-care filling);

7 Calculate total slice conversion *TSC* = _*Wt*×*n*×*l*_;

8 The slices of *SITH* corresponding to top most *TSC*clique members of sorted *Clique List* (*CLCM*) arereplaced with the slices from *SICM*. Modified sliceinfo is *SINEW*;

9 Compute new test pattern*TPNEW* from *SINEW*;

10 Apply clique partitioning heuristic [1] on *TPNEW*;Get resultant*Clique List* (*CLFINAL*) and*Slice Info* (*SIFINAL*) ;Compute final test pattern*TPFINAL* from *SIFINAL*; determine compressionratio of *TPFINAL*; Apply *TPFINAL* to the circuits;compute peak temperature using temperaturecalculation method mentioned in Section IV;pattern sets, one with all the don’t-care bits filled up usingthermal-aware don’t-care bit filling techniques and the otherone is the original test pattern set *TPO* with all the don’tcarebits retained. The test pattern sets with filled don’t-carescan be named as *thermal-aware*

test pattern set (*TPTH*).purpose is to find the final set of test patterns *TPFINAL*with a trade-off between temperature and compression ratio.As no don't-care bit is present in *TPTH*, it cannot use thesuppleness of having don't-care bits, which can be filled upsuitably to increase the number of compatible slices. Hence,it produces a deprived compression ratio. On the other hand, *TPO*gets the full suppleness to fill up the don't-care bits to achieve ahigh compression ratio. Clique partitioning heuristic [1] is practicalon *TPO* to generate a compression-aware *Clique List*(*CLCM*) and corresponding *Slice Info* (*SICM*). The slicesbelonging to *SICM* are called *compression-aware slices* asthe test pattern sets*TPCM* formed from *SICM* produces a goodcompression ratio. The slices obtained from *TPTH* are called*thermal-aware slices* due to their low-temperature consequence.However, these *compression-aware slices* and *therma lawareslices* differ in the procedure of their don't-care bitfilling. A new *Slice Info* (*SINEW*) can be formed takingsome of the *thermal-aware slices* from *SITH* and someof the *compression slices* from *SICM* to have theadvantage of both good compression as well as low temperature.A new set of test patterns is generate using theslice information of *SINEW*. Clique partitioning heuristic [1]is applied on *TPNEW* to get a final clique list *CLFINAL*and matching*Slice Info* (*SIFINAL*). Final test patternset *TPFINAL*, computed from *SIFINAL*,produce a balancebetween compression ratio and temperature. though, thepercentage of *compression-aware slices* that will be therein *SINEW* (with the rest of the *thermal-aware slices*), canbe chosen flexibly using a weightage factor *Wt* with a valuein the range of '0' to '1'. A '0' value of *Wt* chooses allthe *thermal-aware slices*, while a '1' value of it refers to all *compression-aware slices* being chosen. some value between '0' and '1' shows a trade-off between temperature and compression ratio

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VI. EXPERIMENTAL RESULTS AND DISCUSSIONS

In this section, we present the consequences of our thermal-aware test data compression technique on some ISCAS'89 and ITC'99 benchmarks. Temperature planned using the method mentioned in Section IV. Compression ratio (CR) for the dictionary size *D* = 128 for different *NSC* value are shown in the table. *Wt* is varied from '0' to '1' and for each value of *Wt*equivalent temperature in Kelvin (T(K)) and CR (in %)are noted for different *NSC*. It may be noted that, for thevalue of *Wt* = 0, all don't-cares are filled thermally, hence,the test pattern set produces minimum temperature, but theequivalent compression ratio is very poor, while for *Wt*= 1, although the compression ratio is imposing, it producesa high peak temperature, which can be a serious danger tothe thermal safety of the chip. additional values of *Wt* show abalance between compression ratio and temperature. For *Wt*= 0, all the slices being *thermal-aware slices* are expected toproduce minimum temperature. With the gradual increase of*Wt* from '0' to '1', added numbers of *compression-awareslices* replace *thermal-aware slices*, which increase thecompression ratio, but fail to reduce the temperature of thechip. It may be noted that in some cases, the trade-off may notbe offered.

Figure 2 shows a graphical depiction of CR and temperaturefor different values of *Wt* for different scan chainset-ups of benchmark *s*38584. It may be noted from thefigure that temperature increases to a huge extent with theincrease of the value of *NSC*. This is due to transfer ofmore number of test data at a time, which increase transitioncounts in the scan chains and consequently more power consumption.Increasing the number of scan chains may transfer test datafaster dropping test time of the chip, but at the same timeincrease in the temperature may cause permanent damage ofthe chip. However, the difference of CR with *NSC* varies fromcircuit to circuit. Although few benchmarks like *s*13207 and*s*15850 show better compression for larger *NSC*, some otherbenchmark like *s*38417 shows conflicting effect, while for otherbenchmarks CR do not vary much with the increase of *NSC*.Figure

2.Difference of temperature and CR with *Wt* for different scan chainset-up for benchmark *s*38584.As none of the previous compression works report in theliterature have addressed the thermal issue of compression,we could not make a direct comparison of our work withthose. However, our best case CR is similar with theresults presented in [1]. Although some other works attain a better compression ratio with more computationalcomplexity and extra hardware overhead, all are based on theclique partitioning. Method like separating the test slices furtherinto smaller sub-slices can also be included with ourmethod to improve compression ratio without hampering thebalance between CR and temperature of the chip.

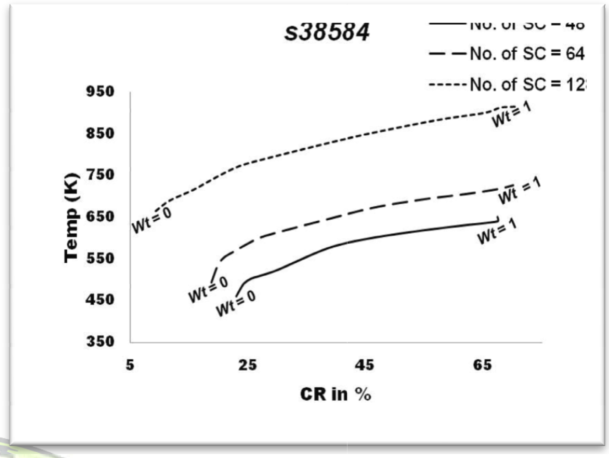

Figure 2.Variation of temperature and CR with Wt for different scan chain set-up for benchmark s38584.

VII. CONCLUSION

The existing technique provide the good compression and temperature reduction. We have proposed a efficient data compression with fast decompression and temperature reduction. The bitmask selection technique significantly reduce the memory requirement.The flexibility of oursystem helps to choose a suitable balance between thermalsafety and test cost to store huge amount of test data.

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