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Design of Efficient Power Reconfigurable Router for Network on Chip (NoC)

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Abstract—Network on chip is an budding technology which provides data consistency and high speed with less power consumption.The router should be designed in a efficient manner as it was a central component of NoC architecture.The components in the router architecture such as buffer,multiplexer,crossbar switch and channels consumes more power. The channel consist of five multiplexer and FIFO buffers.In the proposed paper ,we design reconfigurable router to increase router efficiency in an NoC. The design of the router is done by using verilog Hardware Description Language(VHDL).Xpower analyser tool is used to calculate the total power. The proposed design is simulated by using Modelsim.

Keywords—Network on Chip (NoC) ; Reconfigurable Router; Firstin First out (FIFO) Buffer; Crossbar Switch; Multiplexer.

I. INTRODUCTION

The number of processing elements on a single chip is growing continuously [1]. These processing elements can beprocessors, dedicated Intellectual Property cores (IPs),memory blocks and In/Out communication modules. Thisintegration is called multiprocessor system on chip (MPSoCs)or chip multiprocessors (CMPs) [2]. When the number of Ip cores increases, the conventional type of approaches are not able to provide efficient interconnection. For transferring the data among various IP cores on a single chip require a high performance interconnection. There are several types of interconnections like point to point, bus architecture, Carbon Nanotubes, Optical fiber, and NoCs. Out of these a newparadigm called Network on Chip (NoCs) has been emerged as a replacement to the conventional type of on chip interconnections [3]. In NoCs, large scale networks are scaled down and applied to the embedded system-on-chip (SoCs). Since, large number of IP cores are integrated on a single chip in the NoC design paradigm, the communication among these cores is a dominant issue. Communication among these IP cores should be hassle free. An organized structure is needed to perform this communication. Many types of topologies have been introduced in the literature. The selection of topology is the first task. The NoCs usually have three basics components-routers, links, and wrappers. Router or switch is a very important component of NoCs. The performance improvement, low area, and low power are basic requirements of the router design. The objective of the present work is to design a reconfigurable router for use in NoCs. As a router contains various components like FIFOs, Arbiters etc; the focus is to design components for the low power, low area andhigh performance.

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II. LITERATURE REVIEW

Integrated solutions to demanding design problems in the communications among different IP cores are described in [3].The effect of parallelism on software as well hardware industry and challenges and opportunities in software development based on the current hardware trends are presented in [4]. The implementation of a dynamically reconfigurable NoC router with bus based interface is described in [5]. It also demonstrates the heterogeneous integration of components in NoC architecture and describes about the modeling of reconfigurable components, IP cores and fixed IPs. A novel design approach to customize the routers for reconfigurable systems is presented. It also describes about NOC topology & adjustment of size of the buffers. Clients connected using a modified Fat Tree NoC and its bandwidth requirements are presented in [7]. A dynamic Virtual Channel Regulator (ViChaR) or Unified buffer structure able to dynamically allocate the Virtual Channels (VCs) and buffer resource according to network traffic conditions is proposed in [8]. It also presents the way to maximize the throughput. A complete synthesis flow for customized NOC architectures partitioning
the development work into major steps like topology mapping, selection, and generation and providing tools for their automatic execution is presented in [9]. [10] presents a technique for system-level physical design and interconnection network generation. This approach generates custom low power NOC architectures for application specific SOCs. Wormhole switching with round robin negotiation scheme and dead combination lock free routing for design of a router are described in [11]. A router having eight input ports and one output port for Network on Chip using IP core with latest verification methodologies are presented in [12]. [13] presents the implementation of 5-port 32-bit as well as 64-bit routers using wormhole routing technique for 2D mesh network. Simple deterministic algorithm, flow control and decoding mechanism are used for this purpose. It also discusses about two different types of crossbar switches namely multiplexer and tri-state buffer matrix for efficient design. The router architecture presented in [13] has a fixed and large FIFO size due to which a large FIFO portion is wasted if incoming message has short data length. The size of the FIFO is defined at the design time but its drawback is that it consumes lot of power. Matos [14], proposed a reconfigurable router architecture. Christo Ananth et al. [6] proposed a system, Low Voltage Differential Signaling (LVDS) is a way to communicate data using a very low voltage swing (about 350mV) differentially over two PCB traces. It deals about the analysis and design of a low power, low noise and high speed comparator for a high performance Low Voltage Differential Signaling (LVDS) Receiver. The circuit of a Conventional Double Tail Latch Type Comparator is modified for the purpose of low-power and low noise operation even in small supply voltages. The circuit is simulated with 2V DC supply voltage, 350mV 500MHz sinusoidal input and 1GHz clock frequency. LVDS Receiver using comparator as its second stage is designed and simulated in Cadence Virtuoso Analog Design Environment using GPDK 180nm .By this design, the power dissipation, delay and noise can be reduced.

By reconfiguration process, this architecture uses less number of FIFOs for storing large data.

III. PROPOSED WORK

In this work, we have created some sub-modules to design the complete router. Description about these sub-modules is given below. The HDL code for all the sub-modules is written in Verilog, and then simulated in MODELSIM Edition 10.3. For the Synthesis purpose Xilinx ISE Design Suite 13.4 is used. It provides the RTL view, design summary of circuit, and total power consumption by the circuit. Xilinx SPARTAN-6 FPGAs are used for the implementation.

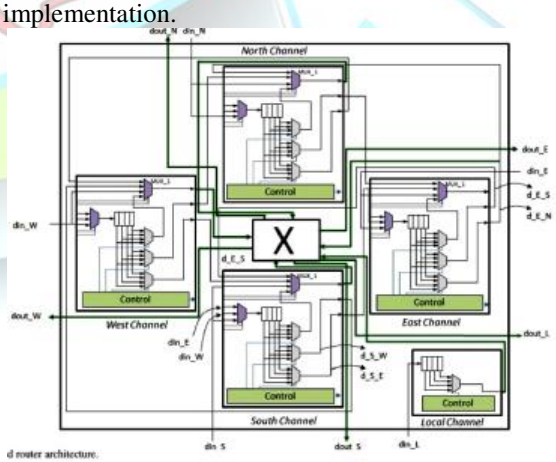

Fig. 1. Router architecture proposed by Matos [14].

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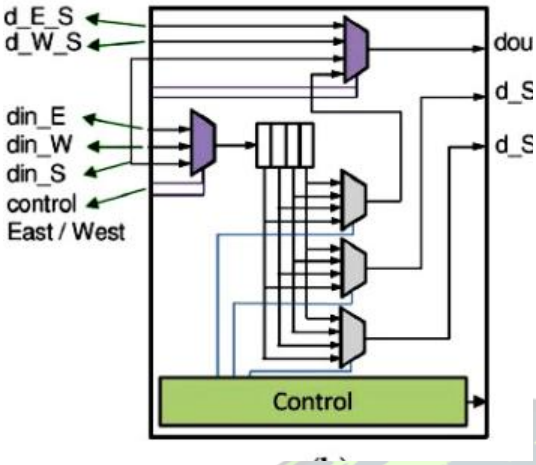

Fig. 2. Input FIFO in South Channel [14].

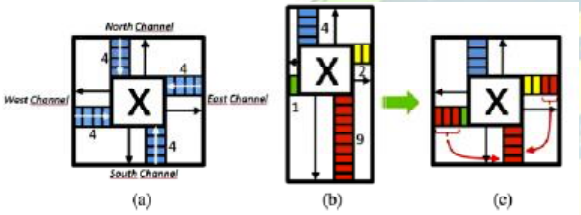

Fig. 3. (a) Design of reconfigurable router with FIFO depth 4 (b) need of the router or according to need of data (c) buffer words distribution among the neighboring channel [14].

A. Design of FIFO

In digital circuits if the source clock is higher than the destination clock, the inability of the destination to sample at the source speed results in loss of data. To remove this problem, high performance parallel interfaces between independent clock domains are made with FIFOs. Each FIFO is controlled by separate clocked read and write signals. A basic FIFO unit with input and output ports is shown in Fig. 4.

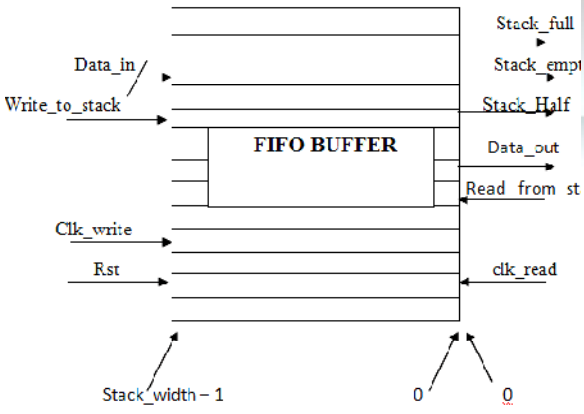

Fig. 4. FIFO buffer unit and input output ports.

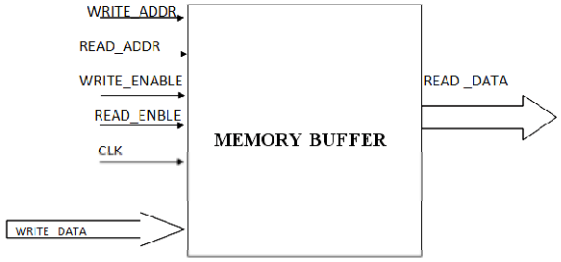

Fig. 5. Memory Array control logic block.

Fig. 5 shows the memory array control logic block. In it, write Control Logic is used to control the write operation of the FIFO's internal memory. Binary-coded write pointer is generated. This pointer points to the memory location where the incoming data is to be written. After every successful write operation the write pointer is incremented by one. It, also generates FIFO full and almost full flags. These flags are used to prevent any loss of data. Similar to the write control logic, the Read control logic is used to control the read operation of the FIFO's internal memory. Binary-coded read

pointer is generated which points to the memory locality from somewhere the data is to be read. After every successful read operation, the Read pointer is incremented by one. Write and read logic control blocks are shown in Fig. 6.

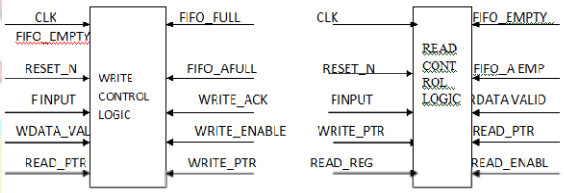

Fig. 6. Write and read logic control blocks.

B. Design of Multiplexer

A multiplexer can use addressing bits to select one of several input bits to the output. A selector chooses a single data input and passes it to the multiplexer output. 4x1 multiplexer implemented from And-Or-Invert (AOI) gates is shown in Fig. 7.

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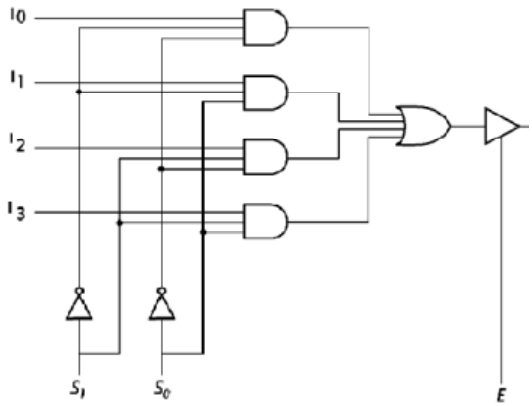

Fig. 7. 4x1 Multiplexer.

C. Design of Crossbar Switch

The heart of the router data path is called the crossbar switch. Mainly router is used for transferring the data between many inputs and many outputs. A crossbar switch also known as matrix switch or cross point switch is used to connect multiple inputs to multiple outputs. The design of crossbar switch used in the present work has 5 inputs and 5 outputs. It switches the data from the input port to the output port during the essence of the router function. The gate level circuit of the cross bar used in the present work is shown in Fig. 8.

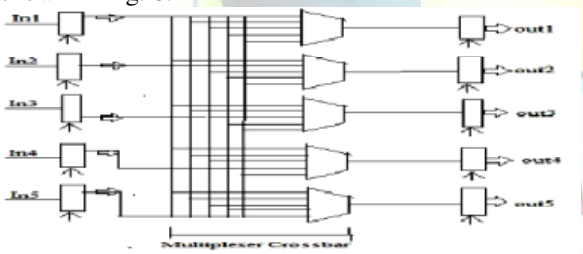

Fig. 8. Multiplexer based crossbar switch for 5 ports [12].

D. Power Analysis using Xilinx Power Analyzer tool (XPA)

Xilinx Power Analyzer (XPA) is a design tool used to analyze real design data. It is used to calculate power after design implemented in Xilinx ISE software. It uses the NCD file output from Place & Route (PAR) step.

E. Power Reduction Technique

Leakage currents along with dynamic currents are the major source of power dissipation in VLSI circuits. To reduce the leakage power an effective technique namely Power gating is used in the present work. This technique is usually used in design of microprocessors. To apply power gating in packetswitched NoCs has specific considerations. Full connectivity is needed to ensure that there are paths for every packet where all the nodes are sending messages periodically. Always-on links can be configured to provide this type of connectivity while other links may be dynamically switched on/off. Fig. 9 shows a segment of a torus network exploiting power gating technique [15].

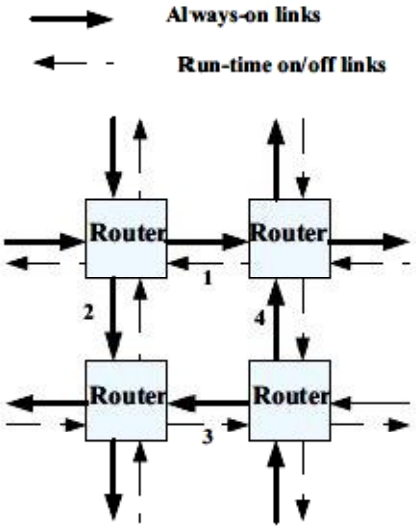

Fig. 9. Exploration of Power-gating technique in NoCs [15, 16]

IV. RESULTS AND DISCUSSION

A. FIFO

Code is written in VERILOG and simulated using Modelsim. By providing some data into FIFO, stack memory locations could be checked. Simulation waveforms of FIFO are shown in Fig. 10. In the simulated waveforms it can be verified that FIFO_ buffer locations or memory locations are occupied by this series of data or not. It can be seen in Fig. that all four memory locations are occupied by a series of data. The code is successfully synthesized using Xilinx ISE 13.4 and the output as the RTL view of FIFO is shown in Fig.11.

B. Multiplexer

Fig. 12 and 13, show the simulated waveform and RTL view of multiplexer.

C. Channel using Crossbar Switch

Output waveform of the complete south channel is shown in Fig. 14. All the four channels are connected to crossbar switch because final output is taken from the crossbar.

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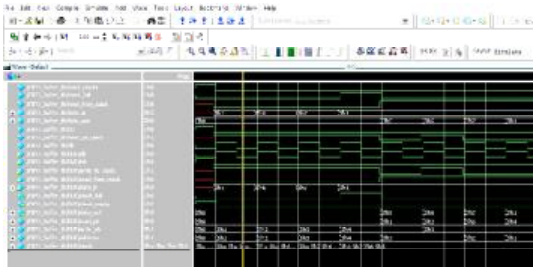

Fig. 10. FIFO waveform.

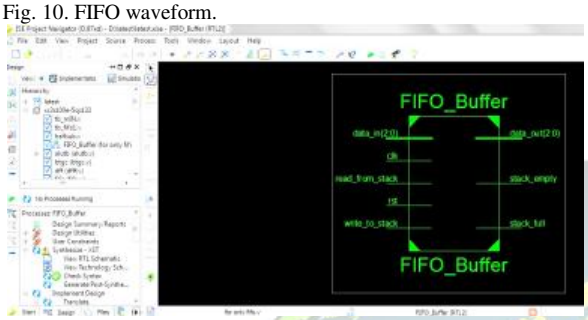

Fig. 11. RTL View of FIFO.

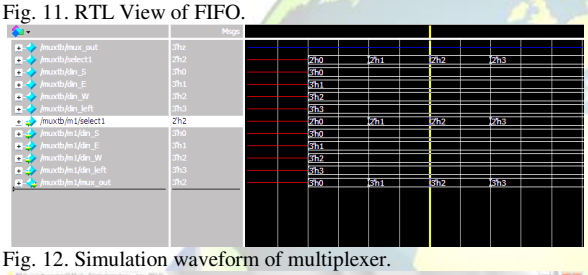

Fig. 12. Simulation waveform of multiplexer.

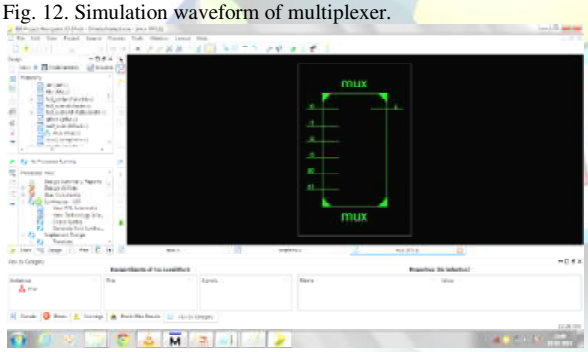

Fig. 13. RTL view of multiplexer.

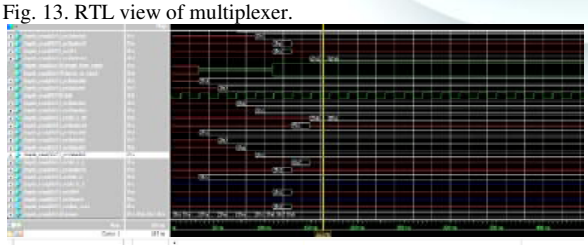

Fig. 14. Complete south channel waveform.

Fig. 15, shows how FIFO buffer of south, west & east occupies by data value. Waveform of store value in South, East, West channels are shown. The stored value of south, east, and west FIFO Stack is shown in Fig. 16. The final output of south channel is taken from the mux5 of south channel, and connected to the crossbar switch.

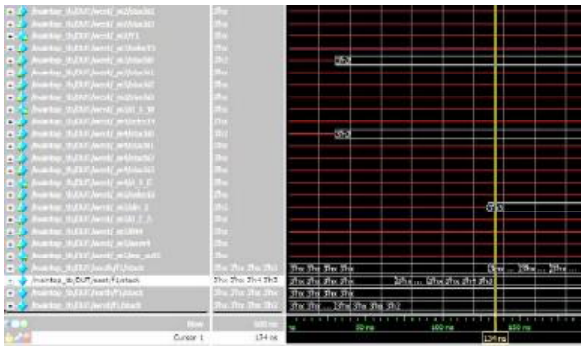

Fig. 15. West FIFO Stack and East FIFO Stack.

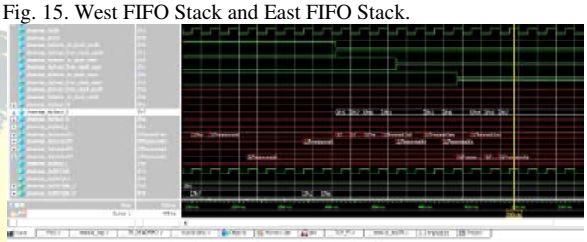

Fig. 16. Waveform of final output dout_S after simulation.

RTL view of the complete architecture is shown in Fig. 17.

All the four channels (south, west, east and north) and the crossbar switch are visible in this diagram. RTL View of complete one channel is shown in Fig. 18. It includes FIFO, five multiplexer and the crossbar.

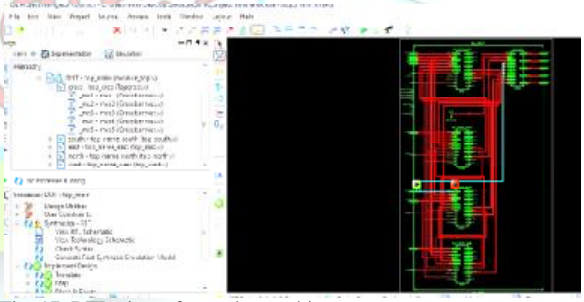

Fig. 17. RTL view of complete architecture.

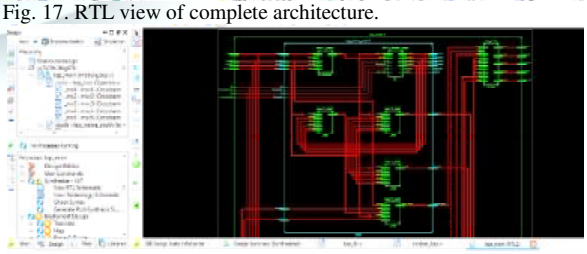

Fig. 18. RTL View of complete one channel.

D. Power Calculation

Calculation of total power dissipation of complete router architecture is done with the help of XPower Analyzer in Xilinx ISE 13.4. For this purpose FPGAs Kit (Spartan-6) is used.Total power without applying

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power gating technique**:** The total power is calculated at a frequency of 100 MHz.Obtained results are shown in Fig. 19. It is obvious from Fig. 19 that total power dissipated by the router architecture is 20 mW.

Total power while applying power gating technique:

Power gating is applied to reduce the total power dissipation of the present architecture. Fig. 20 shows the total reduced power after applying power reduction technique. The comparison of reduced power with total power of router architecture depicts that 5 mW power is reduced after applying the power gating technique.

Fig. 19. Total powers without power reduction technique.

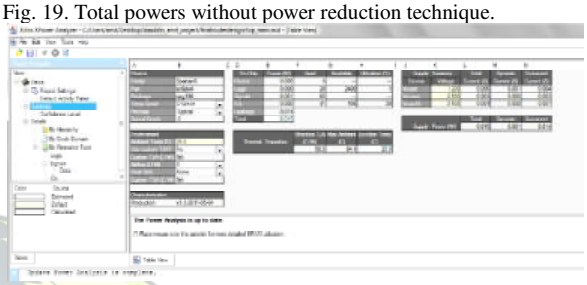

Fig. 20. Total Reduced Power after Applying Power Reduction Technique.

V. CONCLUSION

Router is the most important component of NoCs design. A modified reconfigurable router to be used in NoCs is proposed in the present work with objectives of low power consumption and high performance operation. The proposed router architecture consists of four channels (namely, east, west, north and south) and a crossbar switch. Each channel has First in First out (FIFO) buffers to store the data and multiplexers to control the input and output of data. Stack height of a FIFO buffer is considered to be four and stack width of FIFO is considered to be three. It means it has four locations and each location can store three bit of data. Each channel has five multiplexers. Two multiplexers are used to control the input and output of data and remaining three are utilized to control read and write processes of FIFO. Verilog Hardware Description Language (Verilog HDL) is used for the design entry of this router. For simulation and synthesis MODELSIM EDITION10.3 and XILINX ISE Design Suite 13.4 are used respectively. RTL view of architecture is shown by Xilinx ISE tool. The proposed reconfigurable router is synthesized using Xilinx SPARTAN-6 FPGAs. After Simulation and Synthesis of the proposed router architecture, total power is calculated with the help of XPower analyzer tool. The power gating technique is used to reduce the power dissipation of the proposed reconfigurable router. 5 mW power has been reduced after applying powergating technique in the proposed router architecture compared to the previous architecture.

REFERENCES

[1] ITRS the international technology road map for semiconductors: 2007,"
Available: http://www.itrs.net, pp. 15, 2007.
[2] R. Saleh, S. Wilton, S. Mirabbasi, A. Hu, M. Greenstreet, G. Lemieux, P.P. Pande, C. Grecu and A. Ivanov, "System-on-chip: reuse and integration, " Proceedings of the IEEE, vol. 94, no. 6, pp. 1051-1069, June 2006.
[3] L. Benini and G.D. Micheli, "Network on chips: a new SoCs paradigm," IEEE Computer, vol. 35, no. 1, pp. 70–78, Jan. 2002.
[4] L. Manferdelli, N.K. Govindaraju and C. Crall, "Challenges and
opportunities in many-core computing," Proc. IEEE, vol. 96, no. 5, pp. 808–815, May 2008.
[5] B. Ahmad, A. Ahmadinia, and T. Arslan, "Dynamically reconfigurable NoCs with bus based interface for ease of integration
and reduced designed time," in Proc. NASA/ESA Conf. Adapt. Hardw. Syst. (AHS), pp. 309–314, 2008.
[6] Christo Ananth, Bincy P Chacko, "Analysis and Design of Low Voltage Low Noise LVDS Receiver", IOSR Journal of Computer Engineering (IOSR-JCE), Volume 9, Issue 2, Ver. V (Mar - Apr. 2014), PP 10-18
[7] A. Bouhraoua and M.E. Elrabaa, "Addressing heterogeneous bandwidth requirements in modified fat-tree network-on-chip," in Proc. 4th IEEE Int. Symp. Electronic Des. Test Appl. (DELTA), pp.
486–490, 2008.
[8] C. Nicopoulos, K. Park, D.N. Vijaykrishnan, S. Yousif, and C. Das, "ViChaR: a dynamic virtual channel regulator for networkon-chip routers," in Proc. 39th Annu. Int. Symp. Microarch. (MICRO), pp. 333–346, 2006.
[9] D. Bertozzi, A. Jalabert, M. Srinivasan, R. Tamhankar, S. Stergiou, L. Benini, and G.D. Micheli, "NoCs synthesis flow for customized domain specific multiprocessor systems-on-chip," IEEE
Trans. Parallel Distrib. Syst., vol. 16, no. 2, pp. 113–129, Feb. 2005.
[10] K. Srinivasan and K.S. Chatha, "A low complexity heuristic for design of custom network-on-chip architectures," in Proc. Des., Autom. Test Euro. Conf., vol. 1, pp. 1–6, 2006.
[11] M.L. Swethlana, V. Lavanya, and Dr. R.R. Reddy, "Design and verification eight port router for network on chip," International

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Vol. 3, Special Issue 2, March 2016

Journal of Engineering Research & Technology, vol. 1, pp. 1-5, July
2012.
[12] S. Sahu and H. M. Kittur, "Area and power efficient network on
chip router architecture," IEEE Conference on Information and Communication Technology (ICT), pp. 855-859, April 2013.
[13] M.P. Véstias and H.C. Neto, "A generic network-on-chip architecture
for reconfigurable system: implementation and evaluation," IEEE international conference on field programmable logic and application,
pp. 1-4, Aug. 2006.
[14] D. Matos, C. Concatto, M. Kreutz, F. Kastensmidt, L. Carro and A.
Susin, "Reconfigurable routers for low power and high performance," IEEE Transaction on Very Large Scale Integration (VLSI) System, vol. 19, no. 11, pp. 2045-2057, Nov. 2011.
[15] L. Guang, P. Liljeberg, E. Nigussie and H. Tenhunen, "A review of
dynamic power management methods in NoCs under emerging design considerations," IEEE NORCHIP, pp. 1-6, Nov. 2009.
[16] V. Soteriou and Li-Shiuan Peh, "Exploring the design space of selfregulating
power-aware on/off interconnection networks." IEEE Transactions on Parallel and Distributed Systems, vol. 18, no. 3, pp.
393–408, 2007.