Low Power Design of Reconfigurable Filter Bank for Multi standard Wireless Communication Receivers

Selvi D[1], Sowmiya M[2]

1 2 M.E Communication Systems , Assistant Professor
Department of Electronics and Communication Engineering
Bharathiyar Institute of Engineering for Women
1 2 (selvidharmalingam8@gmail.com) , (r.sowmiyaya@gmail.com)

Abstract: This project presents a plan of linear-phase,low-complexity, reconfigurable digital filter bank that offers independent and entire restraint across the bandwidth as well as the center frequency of each one subbands. The proposed filter bank is designed by integrating spectral parameter approximation (SPA) method with the modified coefficient decimation method (MCDM), referred to as SPA-MCDM-FB. The SPA-MCDM-FB is next merged with the upper confidence bound (UCB)-based decision making algorithm to examine the vacant band(s) of some essential bandwidth for spectrum-sensing application in cognitive radio (CR). We propose to design a Linear Phase FIR Filter using Parallel Distributed Arithmetic Algorithm to reduce the power consumption.

Key terms: spectral parameter approximation (SPA), modified coefficient decimation method (MCDM), upper confidence bound (UCB), cognitive radio (CR), spectrum-sensing.

I. Introduction

Adaptive filters are broadly used in some digital signal course applications. The tapped-linger boundary finite impulse response (FIR) filter whose influences are modernized by the well-known Widrow–Hoff least mean square (LMS) algorithm is the mainly broadly used adaptive filter not only due to its straightforwardness but also due to its adequate convergence carrying out [1].The direct form arrangement on the ahead path of the FIR filter consequence in a long critical route due to an inner-product computation to get a filter production. Therefore, when the data signal has a high sampling rate, it is essential to demote the critical footpath of the structure so that the censorious path could not be more than the sampling time. In recent years, the multiplier-less give out arithmetic

(DA)-based technique [2] has gained considerable fashionableness for its high-throughput processing ability and uniform, which consequence in cost-effective and area–time well efficient computing structures. Hardware-efficient DA-based plan of adaptive filter has been advocate by means of Allred *et al* [3] using two unconnected lookup tables (LUTs) for filtering and weight update. Guo and DeBrunner [5] have recover the design in [3] by using exclusively one LUT for filtering as well as weight upgrade. Although, the structures during [3]–[5] do not endure high sampling rate since they involve a number of cycles for LUT updates for each recently developed sample. In a recent paper, we possess proposed an competent architecture for high-speed DA-based adaptive filter with extremely low adaptation delay [6]. This concise intend a novel DA-based architecture for low power, low-area together with high-throughput conveyor implementation of adaptive filter with extremely low adjustment delay. The contributions of this brief are such as follows.

1) Throughput rate is notably increased by a parallel LUT update.

2) Further improvement of throughput is attained by convergent implementation of filtering along with weight updating.

3) Normal adder-based carry accumulation is replaced by a contingent carry-save accumulation of signed biased internal products to shrink the sampling period. The bit round period amount to ability to remember access moment plus 1-bit full-adder time (Rather of wavelet carry supplement time) by carry-save accumulation.The exercise of the proposed signed carry-save assembling beside helps to reduce the area complication of the proposed pattern.

4) Demotion of power using up is achieved by using a fast bit clock for carry-save accumulation conversely a substantial slower clock for all other operations.

5) The existing designs require gradient auxiliary control component for address generation, which is not required in the proposed structure.

II. Literature survey

In modulation-based filter banks [5], [24], a low pass prototype filter is modulated to obtain multiple bandpass responses with distinct center frequencies. Since there is no need of implementing separate filter for each subband, the modulated filter banks are computationally efficient (i.e., lower hardware cost and multiplication rate). Among the existing modulated filter banks, the discrete Fourier transform filter bank (DFTFB) [5] is widely used uniform filter bank, that is, subband bandwidth is fixed and equal to the passband width of the prototype filter. The coefficient decimation method (CDM)-based reconfigurable CDM-DFTFB in [24] allows coarse control over the subband bandwidth. The modulation-based filter banks are widely used for applications such as channelization when the input signal consists of channels corresponding to single communication standard. However, they cannot provide the subbands of distinct bandwidth and have the constraint of fixed center frequency for each subband, which limits their functionality

when the input signal be composed of channels corresponding multiple communication standards. A new approach of linear-phase reconfigurable filter-bank design is proposed in this paper, which is based on the integration of the Farrow structure [13], spectral parameter approximation (SPA) technique [14]–[18], and modified coefficient decimation method (MCDM) [19]. Hereinafter, it will be referred to as SPA-MCDM-FB which is designed by exploiting architectural advantages of the Farrow structure [13] as well as exclusive multiband response capability of the MCDM [19]. The design example shows that the SPA-MCDM-FB provides an unabridged and independent control over the bandwidth and the center frequency of each subband over the absolute Nyquist band lacking the hardware reimplementation or coefficient updates.

The SPA-MCDM-FB architecture offers substantial savings in total gate count, number of variable multipliers, and group delay over other filter banks. Moreover, these reductions increase furthermore with the increase in the filter-bank resolution (i.e., number of subbands). Christo Ananth et al. [4] proposed a system which contributes the complex parallelism mechanism to protect the information by using Advanced Encryption Standard (AES) Technique. AES is an encryption algorithm which uses 128 bit as a data and generates a secured data. In Encryption, when cipher key is inserted, the plain text is converted into cipher text by using complex parallelism. Similarly, in decryption, the cipher text is converted into original one by removing a cipher key. The complex parallelism technique involves the process of Substitution Byte, Shift Row, Mix Column and Add Round Key. The above four techniques are used to involve the process of shuffling the message. The complex parallelism is highly secured and the information is not broken by any other intruder.

Note that the design of the SPA-MCDM-FB is an extension of our recent work on the design of variable digital filter (VDF) in [18]. In this paper, we make a signification extension of the work in [18] to realize a low-complexity, linear-phase, reconfigurable filter bank along with the architectural details, ate count complexity analysis as well as the demonstrations of superiority of the SPA-MCDM-FB over uniform filter banks [5], [6], [23] for applications such as spectrum sensing and channelization in CRs.

III. Proposed method

We propose to design a Reconfigurable Filter Bank with Complete Control above Subband Bandwidths for Multistandard Wireless Transmission Receivers.

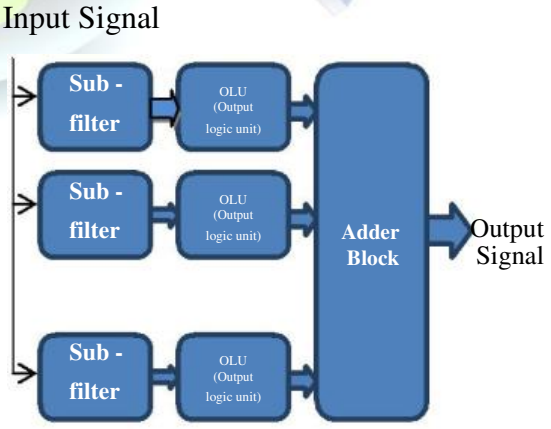


Fig.2.1 Filter Bank Systems

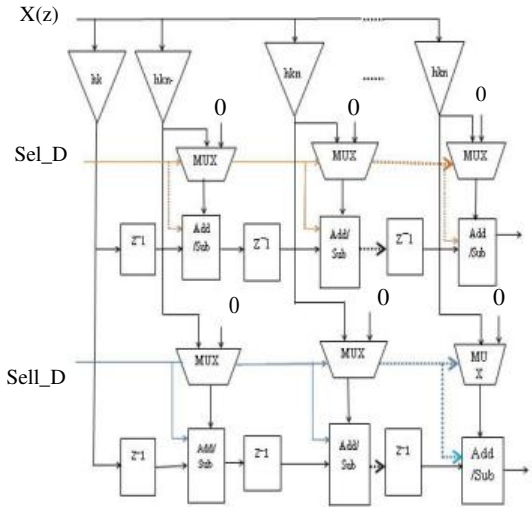


Fig.2.2 **Architecture Of Sub-Filter H(Z)**

The SPA-based VDFs (SPA-VDFs) [14]–[17] are designed using the Farrow structure [13]. The transfer function of the SPA-VDF, $H\alpha(z)$, shown in Fig. 2, is given by [14]–[17]

$H\alpha(z)=\sum_{=0}\sum_{=0} h\ (\ )\ ^{-}\ \alpha_k$ where $hk\ (n)$ is the symmetrical impulse response of Nth-order fixed-coefficient linear-phase subfilters $Hk(z)$, $0 \le k \le L$, and α is the parameter which controls the cutoff frequency of theThe SPA-based VDFs (SPA-VDFs) [14]–[17] are designed using the Farrow structure. The detailed architecture of the kth sub filter where the control signals, sel1_D and sel2_D, select the MCDM factor D for the two branches of these sub filters. The existing modulated filter banks, the distinct Fourier transform filter bank (DFTFB) is broadly used uniform filter bank, The modulation-based filter banks are widely used for applications such as channelization when the input signal consists of channels corresponding to single communication standard.

We propose to design a Linear Phase FIR Filter make use of Parallel Distributed Arithmetic Algorithm.

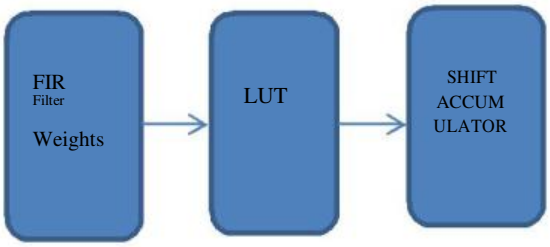


Fig.2.3 FIR Filter Weight Generator

The proposed construction of DA-based adaptive filter of time $N = 4$ is shown in on Fig. 4. It consists of a four-point inner product block and a weight-increment block beside with supplementary circuits for the computation of error value $e(n)$ and control word t for the cask shifters.

The four-point internal-product block [shown in Fig. 5(a)] incorporate a DA table consisting of an group of 15 registers which stores the restricted inner products yl for $0 < l \le 15$ and a 16 : 1 multiplexor (MUX) to pick the gratified of one of those record. Bit piece of weights $A = \{w3l\ w2l\ w1l\ w0l\}$ for $0 \le l \le L - 1$ are fed to the MUX as authority in LSB-to- MSB order along with the output of the MUX is fed to the carry-save accumulator (shown in Fig. 2). Following L bit revolution, the carry-save accumulator shift accumulates all the fragmentary inner products and cause a total word as well as a carry word of size $(L + 2)$ bit each one. The proposed filter-bank design approach looks simple and straight onward, the pattern of the authentic tunable lowpass filter with unabridged control over cutoff frequencies of multiple lowpass responses on entire Nyquist band is an important and challenging research problem.

The carry and sum words are shifted added with an input transmit "1" to initiate filter production which is later subtracted from the specific output $d(n)$ to acquire the error $e(n)$.

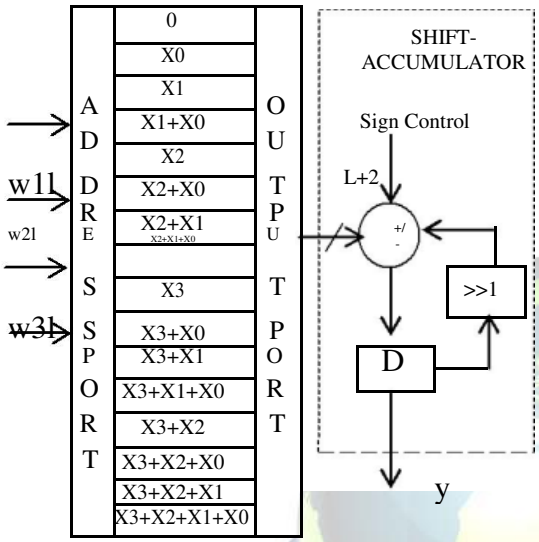


Fig 2.4 Architecture Of Weight Generator

The weight-increment unit for $N = 4$ Consists of four cask shifters and four adder/subtractor prison. The barrel shifter carry the contradictory input values xk for k =0, 1, . . .,N − 1 by appropriate number of locations (intent on by the location of the nearly all significant one in the estimated error). The barrel shifter yields the desired augmentation to be added with or subtracted from the fashionable weights.

The sign bit of the error is familiar with as the jurisdiction for adder/subtractor cells such that, when intimation bit is 0 or one, the barrel-shifter output is appropriate authority with or subtracted from the fulfilled of the realtive current value in the weight register.

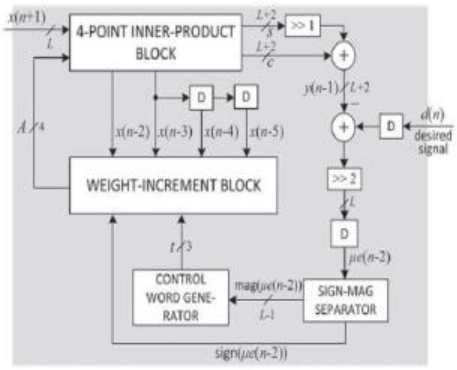


Fig.2.**5** Proposed Structure Of DA-Based LMS Adaptive Filter

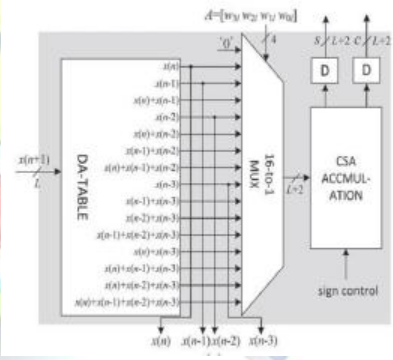


Fig.2.6 Structure of the four-point inner product Chunk

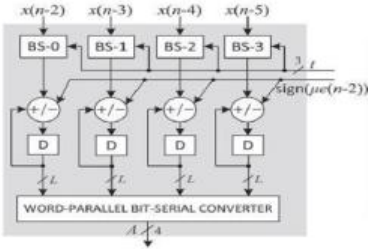
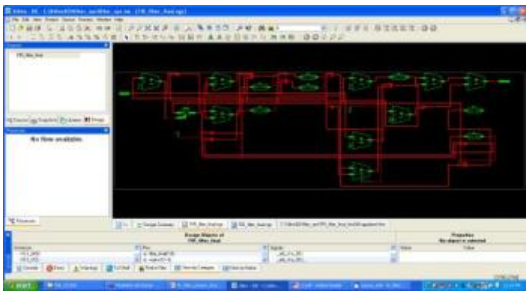


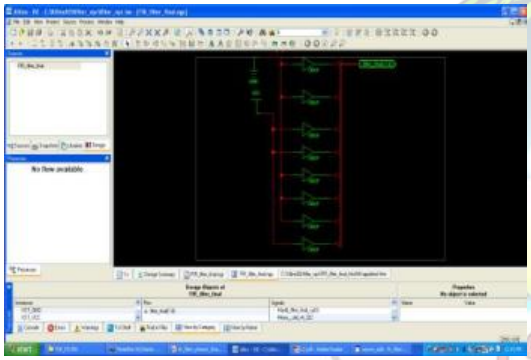
Fig.2.7 Structure of the weight-increment Chunk

III.SIMULATION RESULTS

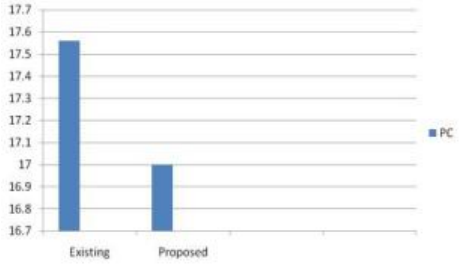
RTL Schematic:



Technology Schematic:



Power Consumption Analysis:



PERFORMANCE ANALYSIS

Performance Evaluation Parameters	Existing Method	Proposed Method
Power consumption	292mW	203mW
Adders	1231	20
Latency	25ns	19.690ns

CONCLUSION

In this paper, a new design of linear-phase reconfigurable filter bank is proposed, which is based on the integration of the Farrow structure, SPA technique and the MCDM, being termed as SPA-MCDM-FB. The applications of the SPA-MCDM-FB for the spectrum-sensing and the channelization tasks in the CRs are also discussed. The design examples demonstrated that the SPA-MCDM-FB provides unabridged and independent control on top of the bandwidth as well as the center rate of occurrence of each subband over the entire Nyquist band. Also, the total gate count, the number of variable multipliers, and the group delay comparisons verified that the SPA-MCDM-FB is higher-ranking compared with alternative linear-phase filter banks. The proposed filter Architecture consumes 203 mW of power consumption,20 number of adders and consumes 19.690ns as latency. We look forward to design a Parallel Linear Phase FIR Filter using Modified Distributed Arithmetic Algorithm with FPGA implementation. Here we exchanging multipliers with adders is superior because adders weight below than multipliers in words of silicon region, and in addition, the

over from the enlarge in adders in preprocessing and post processing blocks remain fixed, not increasing beside accompanied by the distance of the FIR filter, whereas the number of decreased multipliers increases beside with the distance of the FIR filter. To decrease the convolution multipliers in the FIR Filter Architecture, reduce the latency or time cost, Power Consumption, Requires minimum number of gates and LUT's.

REFERENCES

[1] S.Haykin wth B. Widrow, Least-Mean-Square Adaptive Filters. Hoboken, NJ, USA: Wiley, 2003.

[2] S.A. White, "Implementation of the executed arithmetic to digital signal processing and lecture review," IEEE ASSP Mag., vol. 6, no.3, pp. 4–19, July. 1989.

[3] D.J. Allred, H. Yoo, V. Krishnan, W. Huang wth D. V. Anderson, "LMS adaptive filters using distributed arithmetic for giant throughput," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 52, no. 7, pp. 1327–1337, Jul. 2005.

[4] Christo Ananth, H.Anusuya Baby, "High Efficient Complex Parallelism for Cryptography", IOSR Journal of Computer Engineering (IOSR-JCE), Volume 16, Issue 2, Ver. III (Mar-Apr. 2014), PP 01-07

[5] R.Guo with L.S.DeBrunner, "A description of adaptive filter with implementation scheme using dispersed arithmetic," Proc. Asilomar Conf. Signals, Syst., Comput., Comput., Nov. 2011, pp. 160–164.

[6] P. K Meher with S. Y.Park, "excessive-throuhput conveyor consciousness of adaptive FIR filter based on distributed arithmetic," in VLSI Symp. Tech. Dig., Oct. 2011, pp. 428–433.

[7] M. D. Meyer with P. Agrawal, "A integrated pipelined implementation of a delayed LMS transversal adaptive filter," popular Proc. IEEE Int. Symp. Circuits Systems., May 1990, pp. 1943–1946.

[8] J. Mitola with G. Q.Maguire, "Cognitive radio making software receivers more special," IEEE Pers. Commun., vol. 6, no. 4, pp. 13–18, August . 1999.

[9] J. Wang, M. Ghosh with K. Challapali, "Developing cognitive radio application and designs,"IEEE Commun. Mag.,vol. 49, no. 3, pp. 74–81, March. 2011.

[10] D. Feng, C. Jiang, G. Lim, L. J. Cimini, G. Feng with G. Y. Jiang, "A Design of energy-efficient strategy of wireless communications" IEEE Commun. Surveys Tuts., volume. 15, no. 1, pp. 167–178, Feb. 2013.

[11] J. Palicot, H. Zhang with C. Moy, "organized the path to lawn radio," URSI Radio Sci. Bull., no. 347, pp. 40–56, Dec. 2013.

[12] C. W. Farrow, "A continuously fluctuating digital delay element," in Proc. IEEE Int. Symp. Circuits Syst., Espoo, Finland, Junly. 1988, pp. 2641–2645.

[13] S. S. Kidambi, "An efficient closed-form approach to the plan of linear-phase FIR digital filters using variable-bandwidth representative," Signal Process., vol. 86, no. 7, pp. 1656–1669, Oct. 2005.