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Analysis And Implementation Of PI Controller Fordc Link Single Phase PWM Voltage Source Inverter

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Abstract: The Pulse Width Modulation (PWM) DC-to-AC inverter has been widely used in many applications due to its circuit simplicity and rugged control scheme. In the inverters, high-frequency (HF) operation reduces the filter size, which ic claimed to be the biggest advantage. The major limitation in increasing the switching frequency is the switching losses. Hence, zero voltage switching is used to reduce the switching losses. This work proposes a novel controller for enhancing the performance of the inverter. A Zero Voltage Switching (ZVS) DC link single-phase Pulse Width Modulated Voltage Source Inverter (VSI) under open loop and closed loop condition is simulated and presented. Design equations are also discussed and ZVS is achieved for both forward power flow, without increasing the voltage stress on the inverter devices. For the performance evaluation of the proposed converter in closed loop, PI controller is incorporated. The parameters such as output voltage, voltage stress, current through switches and switching losses are obtained and a detailed comparative analysis is made between open loop, closed loop using PI controller.

Keywords: Zero voltage switching, Inverter, Dc link, PI controller, Modulation strategy, Soft switching

I. INTRODUCTION

Switching mode power supplies are widely used in many applications such as uninterruptible power systems, motor drives, induction heating, etc., High-frequency (HF) operation reduces the filter size. The major limitation to increase the switching frequency is the switching losses. Hence, soft switching techniques are used to reduce the switching losses. In the proposed ZVS dc link technique, the switch voltage is clamped to the dc link voltage and PWM schemes can be used to control the inverter output voltage. Soft switching techniques for power inverters have been proposed to improve circuit efficiency, increase power density and reduce voltage and current stresses on the switching devices. Hence, soft switching techniques are used to reduce the switching losses in [1]-[8]. The resonant dc link inverter proposed in [1] has been used to achieve zero-voltage switching (ZVS), but the switch voltage stress is much higher than the dc-link voltage. The inverter proposed in [2] reduces the voltage stress. In [3]–[6] many techniques were proposed to clamp the voltage stress on the switches to dc-link voltage. But they suffer from one or another limitation, like increased complexity due to more number of auxiliary switches, addition of transformer or coupled inductor, complex switching algorithms, etc. Soft switching using auxiliary circuits at the load end has also been proposed in [7]–[8].In [9] used the active circuit in [11]to obtain ZVSof the active switch in a fly back converter. Here the leakage inductance of the transformer is allowed to resonate to obtain soft switching.

But the ZVS is load dependent. The energy stored in the leakage inductance must be sufficient enough to discharge the snubber capacitor of the switch. In [10], a transformer is used **in** the auxiliary circuit to transfer the energy to the output. It reduces the conduction losses but the switching stress and the parasitic oscillations still exists. In [12] the stress across the switch has been reduced. It uses coupled inductance instead of using auxiliary switch. A bidirectional switch [13] is used in the auxiliary circuit to achieve soft switching.

The energy supplied to the split capacitors is not equal. Hence, the voltage levels of the split capacitors differ hence can't achieve soft switching. A rugged soft commutating inverter has been proposed in [13].The inverter could operate efficiently, without voltage. In [12] a new variant of inverter has been proposed for AC drives applications. The presence of resonant capacitor and the clamp diodes substantially reduces the rectifier diode voltage overshoot. In [6] the ZVS using auxiliary circuit was used to obtain soft switching in full bridge dc-dc inverters. And the output voltage has also been controlled to a reasonable extent. The voltage stress has been reduced only to the 15% by using transformer and coupled inductor. But in the proposed work, without the use of transformer and complex coupled inductors, the voltage stress has been reduced to

20% of the dc link voltage. It has been achieved using simple auxiliary switch circuit. Also, the output voltage has also been controlled to a reasonable extent. And, in order to enhance the performance of the inverter for suitable applications and also for increasing versatility, a closed loop controller has been proposed. Closed loop system results has been obtained using PI controller.

II. Block Diagram Of Proposed Inverter

The block diagram of the proposed inverter in closed loop system using controller is shown in Fig.1. There is a Dc link which acts as the interlink between the Dc input and H-bridge inverter. Whenever the input is given as Dc it converts it to Ac as output by means of H-bridge inverter. DC-Link capacitors must be designed for high DC voltages which occur permanently and which may be superimposed with high frequency ripple voltages [2].

The circuit diagram of the proposed DC link single phase PWM voltage source inverter (VSI) is shown in Fig.2.The Proposed inverter consists of a dc link S_{dc} switch, its snubber capacitor C_{dc}, resonant inductor L_r, resonant capacitor C_r, and the H-bridge inverter consisting

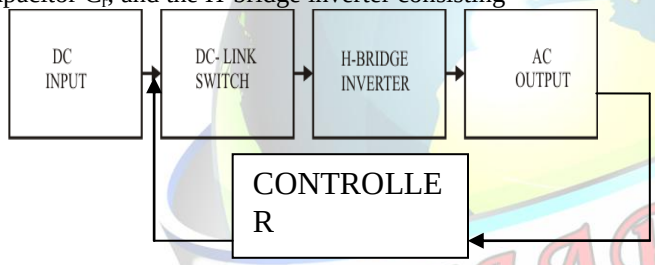

Fig.1.Block diagram of proposed closed loop inverter

of switches S_1,S_2,,S_3,S_4 along with their anti-parallel diodes and snubber capacitors C_1-C_4[1]-[3]. To simplify the analysis, all the components (semiconductor switches, diodes, inductors and capacitors) are assumed ideal [2]. Lagging power factor load is assumed. The load inductance is large enough that the load current is assumed constant in a HF switching cycle.

The H-bridge formed by the switches S_1,S_2,S_3, S_4 performs forward power transfer where S_1-S_2 transfers the power during the positive half-cycle of output and S_3-S_4 transfers the power during the negative half-cycle of output. At which switches S_1,S_3 operates at high frequency (i.e., 50 kHz) and switches S_2,S_4 operates at low frequency (i.e., 50 Hz). The detailed block diagram of the proposed inverter is shown in Fig.3.

Fig.2.Circuit diagram of proposed inverter

Therefore for forward power flow S_i/D_i represents S_1/D_1 or S_3/D_3 during positive half-cycle. Similarly S_a/D_a represents S_4/D_4 or S_2/D_2 during negative half cycle. The capacitor C_s is the snubber capacitance which can be seen in the auxiliary circuit.

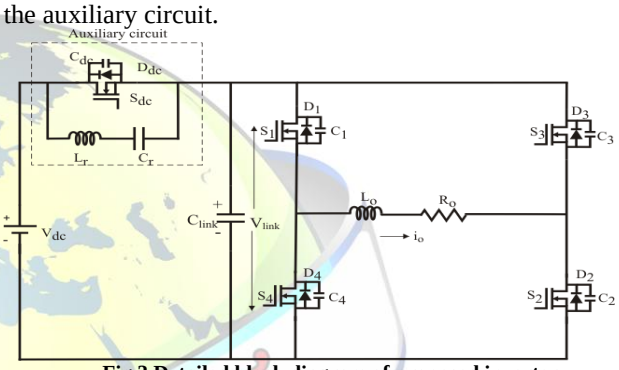

Fig.3.Detailed block diagram of proposed inverter

III.Operating Principle Of Proposed Inverter

A. Circuit Operation

To illustrate the soft switching characteristics of the proposed technique, the operation can be divided in to seven operating intervals. The operating waveforms in different intervals of operation are shown in Fig.4. At the start of the switching period, it is assumed that the equivalent switch S_i is off and the switch S_{dc} is on. The load current is freewheeling through the diode D_a. Let the voltage across the resonant capacitor C_r be V_a. The resonant capacitor is assumed large enough so that the voltage across it is assumed approximately constant, however changes slightly. The inductor current i_{Lr}(i_{Lr}(0-)= -I_a) is flowing through the resonant capacitor C_r and switch $S_{dc.}$ Initially the switch S_{dc} is in ON state. Whenever the supply is given to the circuit the voltage across V_{link} and V_{dc} starts increasing. Then a breach occurs, at a particular instant the voltage starts dropping and reaches zero, at that period the switches S_{dc} and S_1 starts conducting simultaneously. Whenever the voltage across V_{link} comes to zero the switch S_{dc} will starts conduct and whenever the voltage across V_{dc} comes to zero the switch S_1 will starts conducts which has been stated below in the waveforms. Related inductor and capacitor current and voltages have also been shown in Fig.4 and the

equivalent circuits with different operating intervals are given in Fig.5 (a)-(g). The snubber capacitor, C_s starts resonating with the resonant inductor L_r which has been shown in the figure5.a. When the dc bus voltage (V_{Link})reaches zero at t_1 the diode $D_a$starts conducting. The current through L_r(i_{Lr}) linearly rarnps up and reaches –Io at t_a. The switch S_a and S_i are both gated within this interval. The switch S_i turns on with ZVS. The inductor current rises linearly until it reaches the output current I_o.

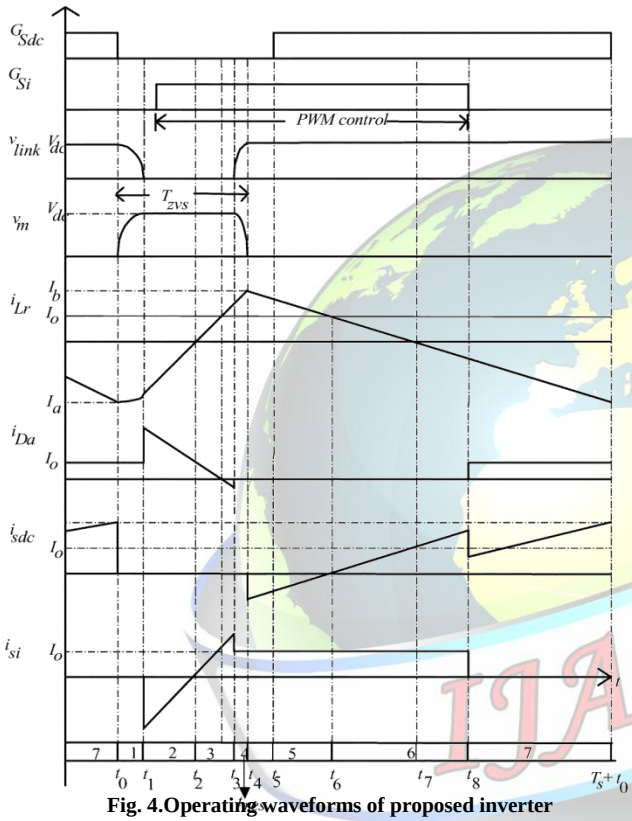

Fig. 4.Operating waveforms of proposed inverter

The diode (D_a)current ramps down and reach zero. Then the reverse recovery current of the diode D_a starts flowing. At the end of this interval the diode stops conducting and enters the blocking mode [4] is shown in figure5.b. The current through L_r continues to increase due to resonance between L_r and C_s. The capacitor C_s is charged until the resonance brings its voltage V_{link} toV_{dc} and the voltage V_m reaches zero is shown in figure5 .c. The blocking voltage of the diode D_a increases and reaches V_{dc}[5]. The circuit diagram depicting this interval of operation is shown in figure5.d. The dc link switch voltage V_m tries to go negative but is clamped by the anti-parallel body diode D_{dc} of the switch, which starts conducting. The switch S_{dc} should be gated within this interval at time t_5(t_4< t_5 <t_6) to obtain zero-voltage turn-on. The resonant inductor current i_{Lr} reaches the output load current value (I_0) at t_6[11]. The circuit diagram depicting this interval is shown in Figure5.e. The dc link switch turns on with zero voltage which is shown in figure5.g. The resonant inductor current i_{Lr} ramps down and reaches zero at t_7 and goes negative, while the dc link switch current increases.

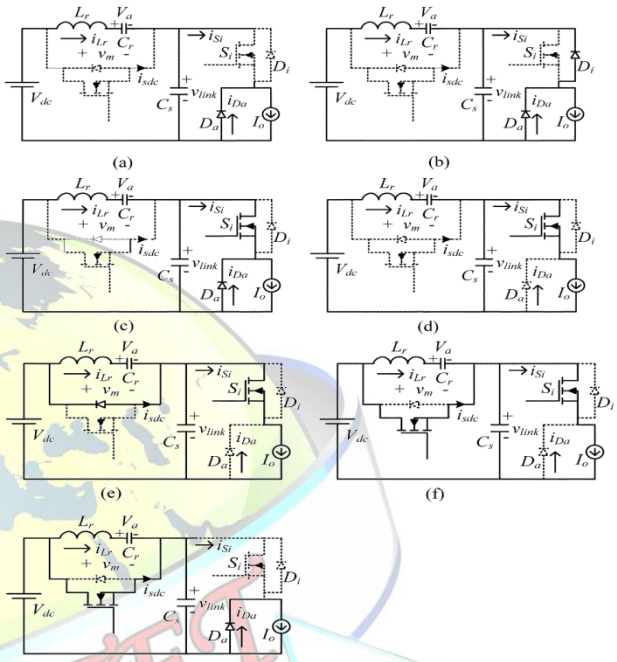

Fig.5.Equivalent circuits during different intervals of the proposed soft-Switched VSI during forward power flow

B. Modulation Strategy

With sine triangle modulation the switching cycle is not synchronized to the carrier at turn-on or at turnoff, i.e., both rising edge and the falling edge are modulated [11].The proposed inverter requires a PWM scheme in which the turn-on of each cycle is synchronized to the carrier (trailing edge modulation). Therefore, the triangular carrier is replaced by a ramp carrier, (Fig.6).

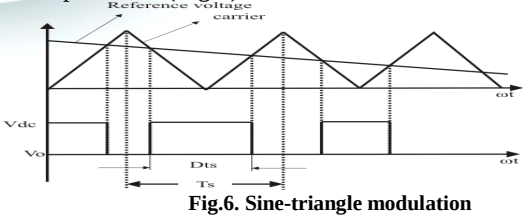

Fig.6. Sine-triangle modulation

With the ramp carrier, the turn-on edge of the switching signal is synchronized to the falling edge of the carrier. The harmonic spectrum of the sine-ramp modulation looks almost same as that of the conventional sine-triangle modulation scheme. During forward power transfer, the

gating signals are obtained from rising ramp-sine modulator (Fig.6) and during reverse power flow; the gating signals are obtained from falling ramp-sine modulator (Fig.7). This can be realized by sensing the inverter bridge output current and obtaining the reverse power-flow regions. Therefore, the triangular carrier is replaced by a ramp carrier (With the ramp carrier, the turn-on edge of the switching signal is synchronized to the falling edge of the carrier. The harmonic spectrum of the sine-ramp modulation looks almost same as that of the conventional sine-triangle modulation scheme.

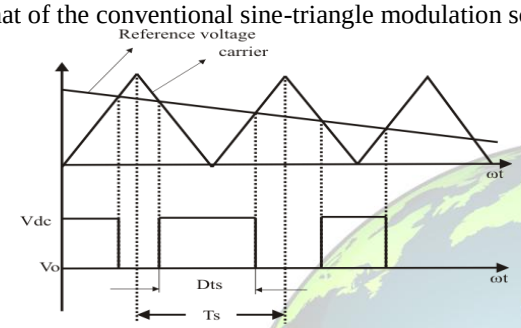

Fig.7. Sine-ramp modulation

C. *Conventional Unipolar Strategy*

The modes of operation in a switching cycle are given in Table.I. The transition from Mode A to Mode B and Mode D to Mode C is with natural ZVS [3], [5]. The transition from Mode B to Mode A and Mode C to Mode D is hard switched. Hence, soft switching mechanisms are required for these transitions. Hence, auxiliary assisted soft switching technique should be applied at Ts for forward power flow and at DT for reverse power flow. This means that the control should detect the point of transfer from Mode C to Mode D so that the auxiliary circuit can be initiated to obtain soft switching. The modes of operation varies depends upon the duration ON period of the switches. The auxiliary switch provides vital role in achieving Zero voltage switching. Since it has single switch instead of transformer and coupled inductor it makes the operation simple. Ts and DT are the parameters which represent the duration of power transfer in forward power flow and reverse power flow respectively which has been shown in Table. I.

TABLE .I. CONVENTIONAL UNIPOLAR SWITCHING SCHEME

Forward Power Flow	
0<t<DTs	DTs<t<Ts
MODE A	MODE B
Power transfer	Power free wheeling
S1-S2 or S3-S4 conduct	S2-D4 or S4-D2 conduct

Hence, soft switching mechanisms are required for these transitions. The control should detect the point of transfer from Mode C to Mode D so that the auxiliary circuit can be initiated to obtain soft switching. Moreover, the auxiliary circuit should reset and get ready as it can be called at any instant between 0 to T_s (duty cycle D will vary along the low-frequency output voltage cycle).The PWM inverter should operate with minimum modulation index so that the auxiliary circuit can be reset.

D. *Modified Unipolar Switching Strategy*

In the modified strategy proposed here, the forward power flow is similar to that of the conventional method. During reverse power flow, the switching cycle starts with power freewheeling and ends with power transfer (different from the conventional control). Table.II presents the modes of operation in a switching cycle. (At the end of the switching cycle for transition from *Mode B* to *Mode A* and Mode *C* to *Mode D). T*he dc link soft switching auxiliary circuits has been activated and the transition is made soft. Hence, the auxiliary circuit will be activated at the end of each switching cycle to obtain ZVS both during forward power flow and reverse power flow [13]. Therefore, the auxiliary circuit has been operated in entire switching period and it must be called for soft transition before getting reseted. During forward power transfer; the gating signals are obtained from rising ramp-sine modulator and during reverse power flow; the gating signals are obtained from falling ramp-sine modulator.

TABLE.II. MODIFIED UNIPOLAR SWITCHING SCHEME

Forward Power Flow	
0<t<DTs	DTs<t<Ts
MODE A	MODE B
Power transfer	Power free wheeling
S1-S2 or S3-S4 conduct	S2-D4 or S4-D2conduct

But this paper deals only with the forward power flow, at which the performance has been improved and their performance parameters were analyzed. It consists of four inverter switches at which upper two switches were operated in higher frequency and lower two switches were operated in lower frequency [11]. They are synchronized by means of multiplexing the both frequencies which produces minimum loss. During forward power transfer, the gating signals are obtained from rising ramp-sine modulator which produces minimum loss. This can be realized by sensing the inverter bridge output current and output voltage.

III. Design Specification

A dc-to-ac bridge inverter with the following specifications has been designed to illustrate the design procedure. Vdc= 220Vdc; output power, $P_{0=}$ 300 VA; output voltage, V_0 =120 Vrms; output frequency, $f_{0=}$ 50 Hz; switching frequency, $f_{s=}$ 50 kHz. The top switches in the full bridge inverter operate at high frequency, while the bottom switches operate at low output frequency.

Hence, MOSFETs are used for bottom switches and for top switches respectively. Moreover, during the forward power freewheeling, the bottom switch diodes are used. MOSFETs with fast anti-parallel diodes are available.

TABLE.III. RESULTS FOR OPEN LOOP SYSTEM

Input voltage	220 V
Input current	2.5 A
Input power	550 W
Output voltage	138 V
Output current	2.45 A
Output power	345 W
Total loss	205 W
Voltage stress	5 V

Fast diodes reduce the circulating energy in the resonant inductor. During R-load the specifications are considered to be Resonant inductor, Lr= 32µH; Resonant capacitor, Cr= 5µF;Snubber capacitor, Cs= 0.333nf; Supply voltage Vdc= 220V; Switching frequency, fs = 50HZ; R load= 60ohm. These specifications can applicable for both R and RL loads respectively.

IV.Results And Discussion

A. *Open Loop System*

The proposed inverter is simulated in MATLAB environment using SIMULINK. An open-loop controller, also called a non-feedback controller, is a type of controller that computes its input into a system using only the current state and its model of the system. A characteristic of the open-loop controller is that it does not use feedback to determine if its output has achieved the desired goal of the input. This means that the system does not observe the output of the processes that it is controlling. Consequently, a true open-loop system can not engage in machine learning and also cannot correct any errors that it could make. It also may not compensate for disturbances in the system. A dc-to-ac bridge inverter with 220V dc input was designed as per design procedure illustrated. The output frequency, is f_o=50 Hz and switching frequency, f_s=50 kHz. The top switches (S_1, S_3), in the full bridge inverter operate at high frequency, while the bottom switches (S_4, S_2) operates at low output frequency. L_r is selected to be 32 mH to limit the di/ dt of the anti-parallel diodes and recovery losses is negligible. Resonant frequency is chosen as f_r=50 kHz and resonant capacitor as C_r=5 µH. The output voltage can be varied from 120v to 140v for the required application and hence the output voltage obtained for open loop system is 138v.

B. *Closed Loop System*

PI controller have two components: the first component, proportional control which generates an output signal proportional to error and second component is integral control, takes into account the error history, and generates output proportional to the integral of error. Proportional controller (Kp) will have the effect of reducing the rise time but, never eliminate the steady-state error [10]. An integral control (Ki) will have the effect of eliminating the steady-state error, but it may make the transient response worse [1]. Effects of each controller parameters kp, and Ki on a closed-loop system are summarized in Table.IV shown below. The PI values are obtained by tuning general inverter transfer function by using MATLAB tuner block.

Fig. 8. Simulation circuit with PI controller

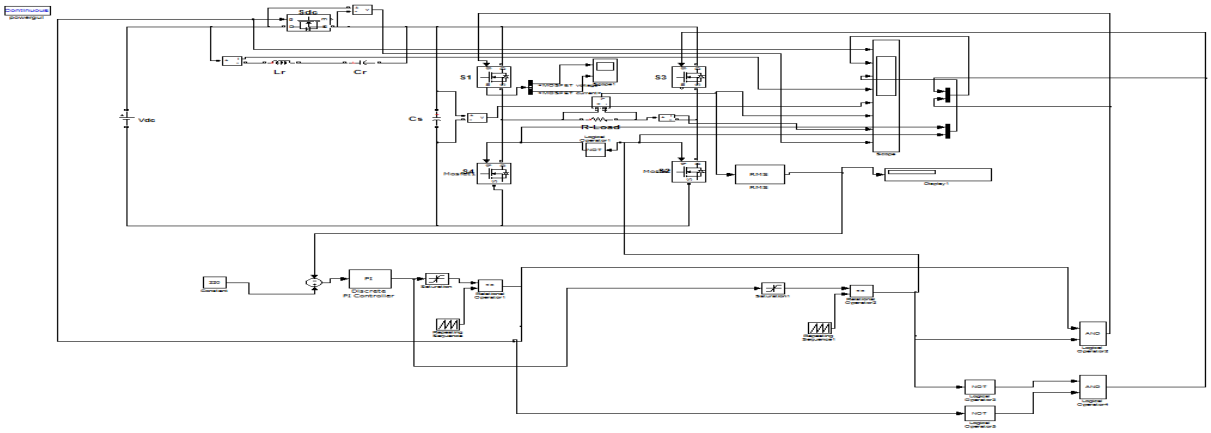

TABLE.IV. TUNED PI VALUES

PARAMETERS	VALUES
Kp	1.2
Ki	0.08

The main simulation circuit of the proposed inverter with PI controller is shown in Fig.8. The following Fig.9 Shows the gate pulses simulated gate pulses for the switchesS_{dc}, S1, S2, S3, andS_4. The switch $S_{dc}$is operated at the frequency of 50 kHz and the switches S_2, S_4 are operated at the frequency of 50HZ. And the switches S_1, S_3 are operated at the frequency by adding the frequencies of 50HZ and 50KHZ respectively.Fig.10 shows the output waveform obtained for PI controller.

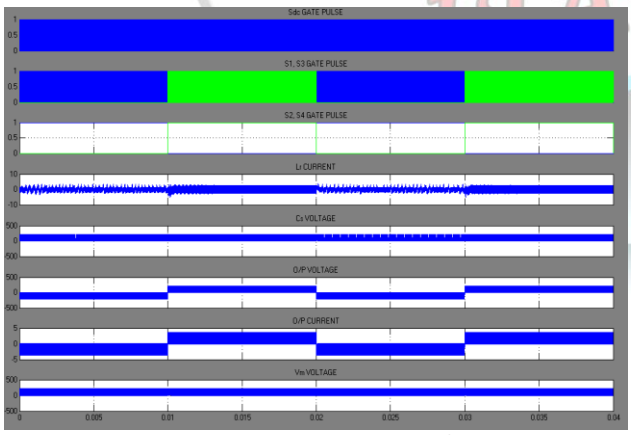

Fig. 9. Simulated output waveforms

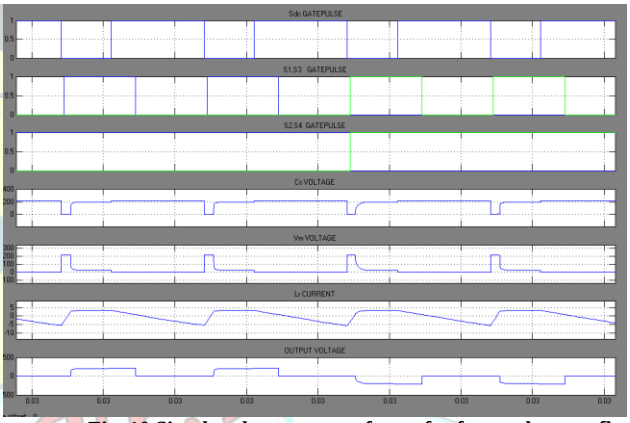

Fig. 10.Simulated output waveforms for forward power flow

V.CONCLUSION

A DC link zero voltage switching single phase Voltage Source Inverter is proposed. The system performance is optimized using the unipolar, sine -ramp modulation scheme. The soft switching for all power factor conditions is achieved. Only one extra switch is required in the dc link to obtain ZVS. Simulation is performed for the proposed inverter for the open loop condition and closed loop condition with PI controller and comparative study is presented. The performance is very much improved in the closed loop system than the open loop system.

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