ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com
International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. II, Special Issue I, March 2015 in association with
SRI RAMANATHAN ENGINEERING COLLEGE, NADUPATTI
International Conference on Recent Trends in Electronics, Communication and Computation Technologies 2015 (ICRTECCT'15)- 5th-6th March 2015

VLSI IMPLEMENTATION OF LOW-POWER ADAPTIVE FIR FILTER USING DISTRIBUTED ARITHMETIC

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ABSTRACT—The main objective is to design DA based adaptive filter in order to decreasing the logic complexity. Throughput is increasedby using parallel Look Up Table (LUT) update and concurrent implementation of filtering and weight-update operations.DA uses bit-serial operations andlook-up tables (LUTs) to implement high throughput filters. Two smart LUT updating methods are developed, and least meansquare (LMS) adaptation is performed to update the weights,and minimize the mean square error between the estimated anddesired output. The conventionaladder-based shift accumulation for DA-based inner-product computationis replaced bycarry-save accumulationin order to reduce the sampling period and area complexity. Reduction of power consumption is achieved in the proposeddesign by using a fast bit clock for carry-save accumulation buta much slower clock for all other operations.

INDEX TERMS—Adaptive Filter, Distributed Arithmetic (DA), FiniteImpulse Response (FIR), Least Mean Square (LMS), Look-Up Table(LUT), Multiply-Accumulate (MAC), Offset-Binary Coding (OBC).

1 INTRODUCTION

Most portable electronic devices, such as cellular phones,PDAs, and hearing aids, require digital signal processing(DSP) for high performance. Due to the increased demandof implementation of sophisticated DSP algorithms, low-costdesigns, i.e., low-area and low-power cost, are needed to makethese hand-held devices small with good performance.Various types of DSP operations are employed in practice.Filtering is one of the most widely used complex signalprocessing operations [1]. For discrete Finite Impulse Response(FIR) filters, the output y(n) is a linear convolution of weightsw_n, and inputs. For an N-order FIR filter, the generation ofeach output sample y(n) takes N + 1 Multiply-Accumulate(MAC) operations. Since general purpose multipliers require significant chip area,

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alternate methods of implementing multiplication are often used particularly when the coefficients values are known prior to implementation.

ADAPTIVE filters are widely used in several digital signalprocessing applications. The tapped-delay line FiniteImpulseResponse (FIR) filter whose weights are updated by thefamousWidrow–Hoff Least Mean Square (LMS) algorithm is themost popularly used adaptive filter notonly due to its simplicity but also due to its satisfactory convergence performance [2].Distributed arithmetic(DA) is one way to implementconvolution multiplier-less,where the MAC operations are replaced by aseries of LUTaccesses and summations. Techniques, such as ROM decomposition [3] and offset-binary coding (OBC) [4] can reducethe LUT size.

2 OVERVIEW OF LMS ADAPTIVE ALGORITHMS

During each cycle, the LMS algorithm computes a filteroutput and an error value that is equal to the difference betweenthe current filter output and the desired response. The estimatederror is then used to update the filter weights in every trainingcycle.

$$\mathbf{W(n+1) = w(n) + \mu \, . \, e(n) \, . \, x(n)} \quad \textbf{(1a)}$$

$$\mathbf{W(n+1) = w(n) + \mu \, . \, e(n-m) \, . \, x(n-m)} \quad \textbf{(1b)}$$

Where,

$$\mathbf{e(n)=d(n) - y(n)} \quad \textbf{(1c)}$$

$$\mathbf{y(n)= w^{qT}(n) \, . \, x(n)} \quad \textbf{(1d)}$$

The input vector $\mathbf{x}(n)$ and the weight vector $\mathbf{w}(n)$ at the $n$thtraining iteration are respectively given by,

$$\mathbf{x(n) = [x(n), x(n-1),\ldots\ldots, x(n-N+1)]^T} \quad \textbf{(2)}$$

$$\mathbf{w(n)=[w_0(n), w_1(n),\ldots\ldots, w_{N-1}(n)]^T} \quad \textbf{(3)}$$

3 EXISTING CONVENTIONAL DA-BASED IMPLEMENTATION APPROACH FORINNER-PRODUCT COMPUTATION

The LMS adaptive filter, in each cycle, needs to perform aninner-product computation which contributes to the most of thecritical path. For simplicity of presentation, let the inner productis given by,

$$= \quad [\ ] \, . \, [\ ] \quad \textbf{(4)}$$

Where c[n] and x[n]for $0 \le n \le N - 1$ form the N-point vectorscorresponding the current weights and most recent$N - 1$ input,respectively. Assuming Bto be the bit width of the weight,each component of the weight vector may be expressed in two'scomplement representation

$$[\ ] = - [\ _0] + \sum \quad [\ _b] \, . \, 2^{-1} \quad \textbf{(5)}$$

wherex_{nb}denotes the bth bit of x_n. Substituting (5), we canwrite (4) in an expanded form

$$\mathbf{y = -\sum \quad [\ _0] \, . \, [\ ] + \sum \quad ^{-b} \quad .\sum \quad [\ _l] \, . \, c[n]} \quad \textbf{(6)}$$

The inner product given by (7) can be computed as

$$\mathbf{y = \sum \quad ^{-b} \, . \, y_l - y_0,} \quad \textbf{(7)}$$
$$\mathbf{where \ y_l = \sum \quad [n] \, . \, x[n_l]}$$

Since any element of the N-point bit sequence $\{x[n_l]$for $0 \le n \le N - 1\}$can either be zero or one, the partial sum ylfor$l = 0, 1, \ldots, L - 1$ can have $2N$ possible values. If all the $2N$possible values of $y_l$are

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pre-computed and stored in a LUT, thepartial sums y_l can be read out from the LUT using the bitsequence $\{xn_l\}$as address bits for computing the inner product .

The inner product of (7) can therefore be calculated in Lcycles of shift accumulation, followed by LUT-read operationscorresponding to Lnumber of bit slices $\{xn_l\}$for $0 \le l \le L-1$, as shown in Fig. 1

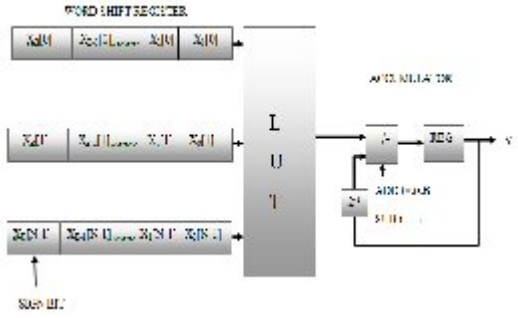

FIG:1 Conventional DA based implementation of four – point inner product

Since the shift accumulation inFig. 1 involves significant critical path, we perform the shiftaccumulation using carry-save accumulator, as shown in Fig. 2.The bit slices of vector **w** are fed one after the next in the LeastSignificant Bit (LSB) to the Most Significant Bit (MSB) orderto the carry-save accumulator. However, the negative (two'scomplement) of the LUT output needs to be accumulated incase of MSB slices. Therefore, all the bits of LUT output arepassed through XOR gates with a sign-control input which is setto one only when the MSB slice appears as address

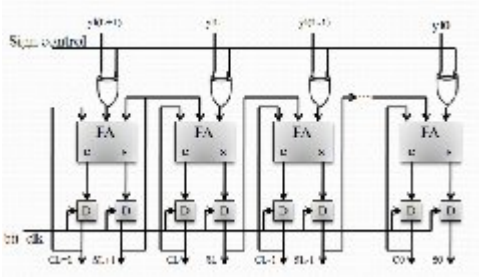

FIG:2 Carry – save implementation of shift accumulation

The XORgates thus produce the one's complement of the LUT outputcorresponding to the MSB slice but do not affect the output forother bit slices. Finally, the sum and carry words obtained after$L$ clock cycles are required to be added by a final adder, and the input carry of the final adder isrequired to be set to one to account for the two's complementoperation of the LUT output corresponding to the MSB slice.

4PROPOSED DA-BASED ADAPTIVE FILTER STRUCTURE FOR N=8 BIT

The computation of adaptive filters of large orders needs tobe decomposed into small adaptive filtering blocks.since DAbasedimplementation of inner product of long vectors requires a very large LUT [5].The proposed structure of DA-based adaptive filter of length$N = 8$ is shown in Fig. 3. It consists of a four-point innerproductblock and a weight-increment block along with additionalcircuits for the computation of error value $e(n)$ andcontrol word t for the barrel shifters.

The four-point inner-product block [shown in Fig. 4]includes a DA table consisting of an array of 15 registerswhich stores the partial inner products $yl$for $0 < l \le 15$ anda 16 : 1 multiplexer (MUX) to select the content of one ofthose registers. Bit slices of weights $A = \{w3l\ w2l\ w1l\ w0l\}$for $0 \le l \le L-1$ are fed to the MUX as control in LSB-to-MSB order, and the output of the MUX is fed to the carry-saveaccumulator (shown in Fig. 2).

As in the case in [5], all the bits of the error except the mostsignificant one are ignored, such that multiplication of input$x_k$by the error is implemented by a right shift through thenumber of locations given by the number of leading zeros in

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themagnitude of the error. The magnitude of the computed error isdecoded to generate the control word *t* for the barrel shifter.The logic used for the generation of control word *t* to be usedfor the barrel shifter is shown in Fig. 5.

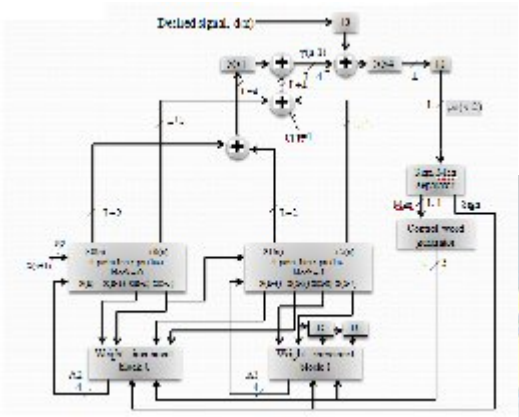

FIG:3 Proposed structure of DA-based LMS adaptive filter of length $N = 8$.

The weight-increment unit [shown in Fig. 6] for $N = 4$ consists of four barrel shifters and four adder/subtractor cells.The barrel shifter shifts the different input values $x_k$for k=0, 1, . . .,N − 1 by appropriate number of locations (determinedby the location of the most significant one in the estimatederror). The barrel shifter yields the desired increments tobe added with or subtracted from the current weights. The signbit of the error is used as the control for adder/subtractor cellssuch that, when sign bit is zero or one, the barrel-shifter outputis respectively added with or subtracted from the content of thecorresponding current value in the weight register.

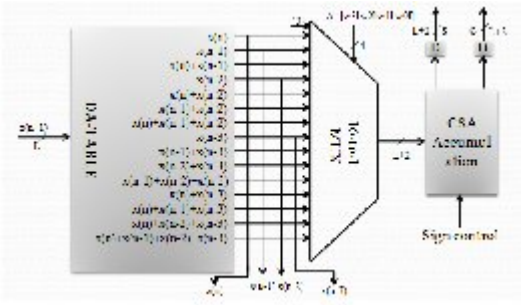

FIG:4 Structure of the four-point inner-product block for N=4

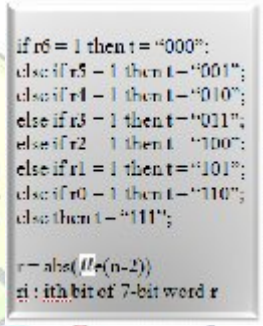

FIG:5 Logic used for generation of control word *t* for the barrel shifter.

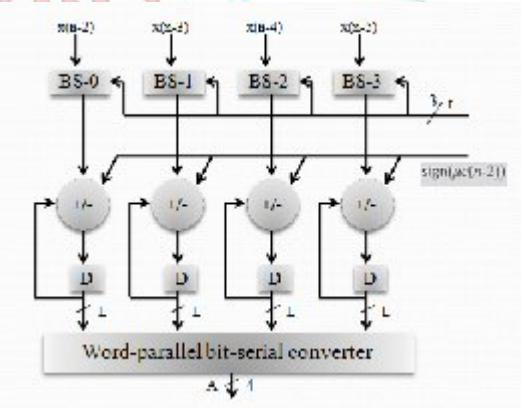

FIG:6 Structure of the weight-increment block for $N = 4$

5SIMULATION RESULTS

5.1CONVENTIONAL DA BASED IMPLEMENTATION

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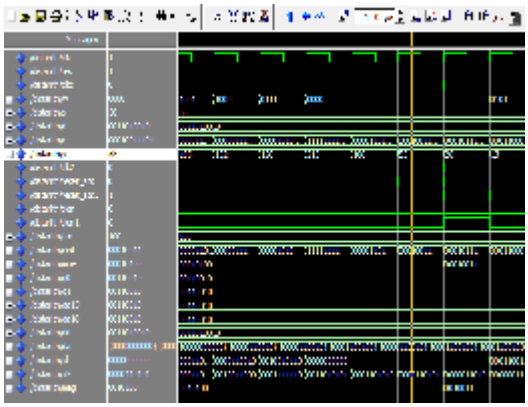

FIG:7 Simulation of Conventional method(N=8)

5.2CONDITIONAL CARRY - SAVE ACCUMULATION DA BASED IMPLEMENTATION

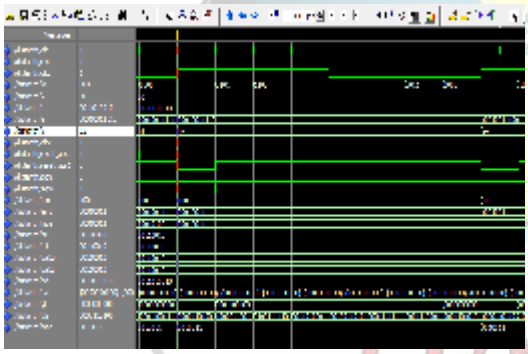

FIG:8 Simulation of Conditional carry save accumulation method(N=8)

6 SYNTHESIS RESULTS

6.1 ESTIMATED POWER FOR CONVENTIONAL METHOD

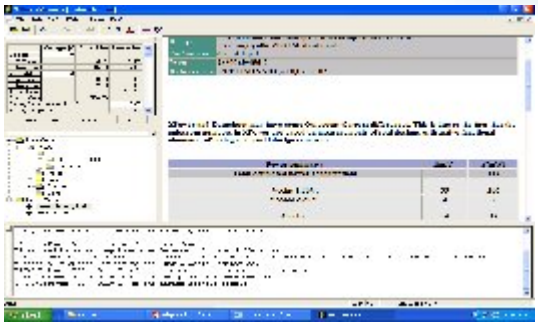

FIG:9Synthesize power for Conventional method(N=8)

6.2 ESTIMATED POWER FOR CONDITIONAL CARRY - SAVE ACCUMULATION METHOD

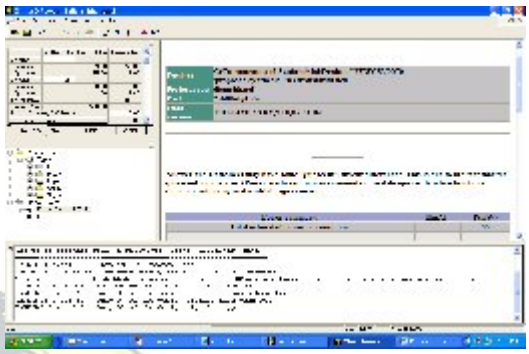

FIG:10Synthesize power for Conditional carry – save accumulation method(N=8)

6.3 ESTIMATED AREA FOR CONVENTIONAL METHOD

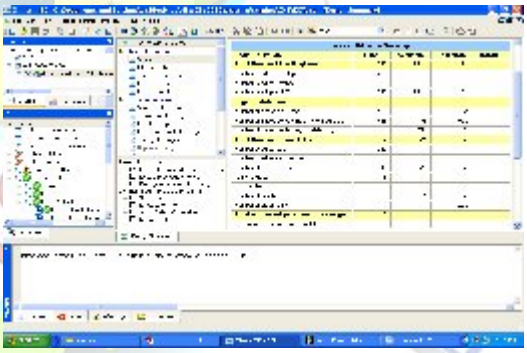

FIG:11 Synthesize area for Conventional method(N=8)

6.4 ESTIMATED AREA FOR CONDITIONAL CARRY-SAVE ACCUMULATION METHOD

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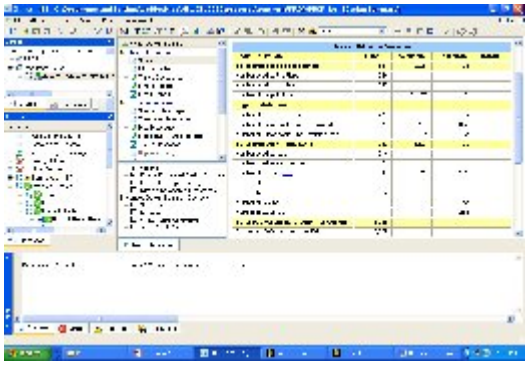

FIG:12Synthesize area for Conditional carry – save

Table 6.1 Comparison for synthesis results

PARAMETERS	EXISTING	PROPOSED
NUMBER OF LUT'S	767	714
NUMBER OF OCCUPIED SLICES	499	475
GATE COUNT FOR DESIGN	9431	9236
POWER CONSUMPTION	112(mW)	86(mW)

7 CONCLUSION

An efficient pipelined architecture for low-power, high-throughput, and low-area implementation of DA-based adaptive filter. Throughput rate is significantly enhanced by parallel LUT update and concurrent processing of filtering operation and weight-update operation. andalso proposed a carry-save accumulation scheme of signed partial inner products for the computation of filter output. From the synthesis results, we find that the proposed design consumes 13% less power and 29% less Area over our previous DA-based FIR adaptive filter in average for filter lengths N = 8 bit. Compared to the best of other existing designs, our proposed architecture provides 9.5 times less power and 4.6 times less Area. Offset binary coding is popularly used to reduce the LUT size to half for area-efficient implementation of DA [4], [8], which can be applied to design as well.

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