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IMPROVING THE POWER QUALITY WITH THE DESIGN OF MULTI CONVERTER UNIFIED POWER QUALITY CONDITIONER (MC-UPQC)

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ABSTRACT: In this project we are implementing the Unified Power Quality conditioner (UPQC) which is connected three phase four wire system. Therefore neutral current will flow toward transformer neutral point which is compensated. During all operating conditions the series transformer neutral must been at the virtual zero potential. Therefore by utilizing the simulation we can verify the power quality problems like unbalance current and voltage and harmonics which is connection non linear load up to three phases four wire with the Unified Power Quality conditioner. By analysis control strategy like unit vector template which is utilized by the series APF to balance the unbalanced current present in the load currents with the detailed concept of single phase PQ theory. By using the simulation results we can handle the function of the UPQC.

INTRODUCTION

As indicated by the expanding use of the nonlinear and electronically exchanged gadgets with the conveyance frameworks and ventures and power-quality (PQ) issues like flicker, harmonics, and imbalance which is serious noticed. More finished by the lightning strikes on transmission lines and exchanging of capacitor banks alongside different system shortcomings which is cause by the PQ issue like voltage swell/sag, interference and transient.

This might be important to compensation. Present day arrangements can be found as dynamic correction or dynamic shifting [2]. A shunt dynamic power channel is reasonable for the concealment of negative load effect on the supply arrange, however in the event that there are supply voltage imbalance, an arrangement dynamic power channel might be expected to give full compensation

As per the current years, arrangements in view of flexible ac transmission systems (FACTS) have showed up. The utilization of FACTS ideas in conveyance frameworks has brought about another age of repaying gadgets. Network as opposed to control the power stream of a solitary line by, for example, an UPFC.

The GUPFC consolidates at least three shunt arrangement converters. It broadens the idea of least difficult GUPFC comprises of three converters—one associated in shunt and the other two in arrangement essential GUPFC can control add up to five power framework amounts, for example, a transport voltage and free dynamic and responsive power streams of two lines. As indicated by the idea of GUPFC can be reached out for more lines if important. The gadget might be introduced in some focal substations to oversee control streams of multi lines or a gathering of lines and give voltage bolster also. By utilizing GUPFC gadgets, the exchange capacity of transmission lines can be expanded altogether.

As indicated by the idea can be reached out to outline multi-converter arrangements for PQ change in nearby feeders. For instance, the interline unified power flow controller (IUPQC), which is the augmentation of the IPFC idea at the dispersion level, has been proposed in [11]. The IUPQC comprises of one arrangement and one shunt converter. In this paper, another design of an UPQC called the multi-converter unified power flow controller (MCUPQC) is introduced. The framework is stretched out by including an arrangement VSC in a nearby feeder.

PROPOSED MC-UPQC SYSTEM

A. Circuit Configuration

The single-line diagram of a distribution Feeder1 from one substation supplying load L1 and feeder2 from another substation supplying load L2 are connected to MC-UPQC through BUS1 and BUS2.

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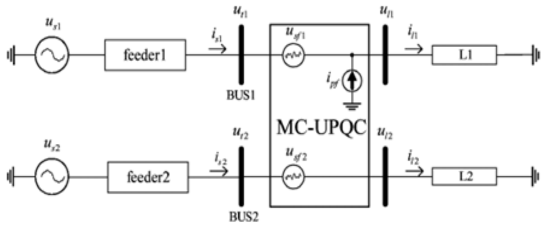

Fig.1. Single-line diagram of a distribution system with an MC-UPQC.

There may be sag/swell in the bus voltages they may get distorted as well.

B. MC- UPQC Structure

The internal structure of MCUPQC consists of three VSCs which are connected back to back through a common dc link capacitor. In the proposed configuration at the end offeeder1, VSC1 is connected in series withBUS1 through a series transformer and VSC2 is connected parallel with load L1 through a shunt transformer; while VSC3 is connected in series with BUS2through a series transformer at the end of Feeder2.

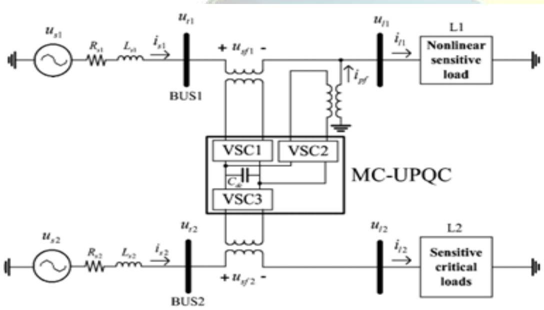

Fig. 2. Typical MC-UPQC used in a distribution system

Each VSC in Fig.2 is realized by a three-phase converter through a commutation reactor and high-pass output filter as shown in Fig. 3.

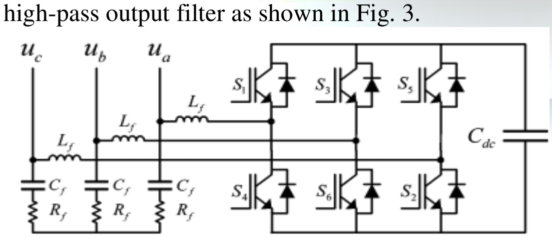
Fig. 3. Schematic structure of a VSC.

The commutation reactor and high pass output filter are connected to prevent the flow of switching harmonics into the power supply. As shown in Fig.2, common dc link capacitor supplies all converters through a transformer is connected to the distribution system. Secondary (distribution) sides of the two series-connected transformers are directly connected in series with BUS1 and BUS2, and the secondary (distribution) side of the shunt connected transformer is connected in parallel with load L1. The goals of the MCUPQC shown inFig.2 areas follow:

1) Load voltage regulation against sag/swell and disturbances intersystem in order to protect the nonlinear sensitive load L1;
2) Load voltage regulation against sag/swell, interruption, and disturbances in the system in order to protect the sensitive critical load L2;
3) To provide compensation for reactive and harmonic components of nonlinear load current.

C. Control Strategy

MCUPQC consists of two series VSCs, one shunt VSC which are operated independently, depending on the control scheme. The switching control strategy for series VSCs uses sinusoidal pulse width modulation (SPWM) voltage control technique while shunt VSC uses hysteresis current control technique respectively. Details of the control algorithm are based on the method [12].

Shunt-VSC: Functions of the shunt-VSC are:
1) Compensate for the reactive component of load L1 current;
2) Compensate for the harmonic components of loadL1 current;
3) To regulate the voltage of the common dc link capacitor.

$$i_{l\_dqo} = T_{abc}^{dqo}\, i_{l_{abc^*}} \quad (1)$$

where transformation matrix is shown in (2), at the bottom of the page.

$$T_{abc}^{dqo} = \frac{2}{3}\begin{bmatrix} \cos(\omega t) & \cos(\omega t - 120^0) & \cos(\omega t + 120^0) \\ -\sin(\omega t) & -\sin(\omega t - 120^0) & -\sin(\omega t + 120^0) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \quad (2)$$

All harmonic components are transformed into fundamental frequency shift a components.

$$i_{l\_d} = \bar{\imath}_{l\_d} + \tilde{\imath}_{l\_d} \quad (3)$$

$$i_{l\_q} = \bar{\imath}_{l\_d} + \tilde{\imath}_{l\_q} \quad (4)$$

Where i_{l_d}, i_{l_q} are dq components of load current, $\bar{\imath}_{l\_d}, \bar{\imath}_{l\_d}$ are dc components,

$$i_{pf\_d}^{ref} = \tilde{\imath}_{l\_d} \quad (5)$$

$$\mathrm{i}_{\mathrm{pf\_q}}^{\mathrm{ref}} = \mathrm{i}_{\mathrm{l\_q}} \quad (6)$$

The feeder current dq components are given by

$$i_{s\_d} = \bar{\imath}_{l\_d} \quad (7)$$

$$i_{s\_d} = 0 \quad (8)$$

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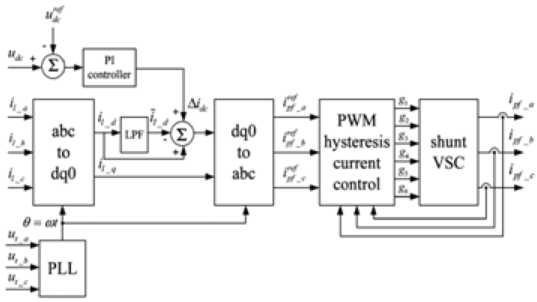

Fig. 4. Control block diagram of shunt VSC.

The input of the PI controls the error between the actual capacitor voltage and its reference value. Anew reference current is obtained by adding output of the PI controller to the shunt-VSC reference current component. Thus the reference current becomes:

$$\begin{cases} i_{pf\_d}^{ref} = \tilde{i}_{l\_q} + \Delta i_{dc} \\ i_{pf\_q}^{ref} = i_{l\_q} \end{cases} \quad (9)$$

As shown in Fig. 4, reference current in (9) is then transformed back into the reference frame. By using PWM hysteresis current control, the output-compensating currents in each phase are obtained

$$i_{pf\_abc}^{ref} = T_{dqo}^{abc} i_{pf\_dqo}^{ref}; \left(T_{dqo}^{abc} = T_{abc}^{dqo-1}\right). \quad (10)$$

Series-VSC: Functions of the series VSCs in each feeder are:

1) Mitigation of voltage sag and swell;

2) Compensation of voltage distortions like harmonics;

3) Compensation of interruptions (in Feeder2 only).

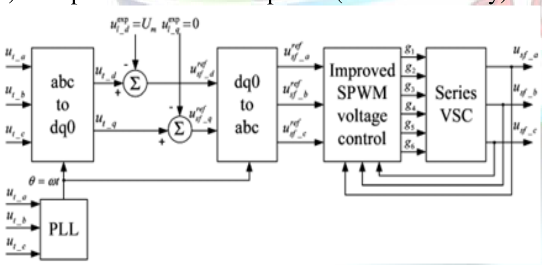

Fig. 5. Control block diagram of the series VSC.

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$$U_{t\_dqo} = T_{abc}^{dqo} u_{t\_abc} = u_{t1p} + u_{t1n} + u_{t10} + u_{t\square} \quad (11)$$

Where

$$\begin{cases} u_{t1p} = [u_{t1p-d} \quad u_{t1p-q} \quad 0]^T \\ u_{t1n} = [u_{t1n-d} \quad u_{t1n-q} \quad 0]^T \\ u_{t10} = [0 \quad 0 \quad u_{00}]^T \\ u_{t\square} = [u_{t\square-d} \quad u_{t\square-q} \quad u_{t\square\_}]^T \end{cases} \quad (12)$$

$u_{t1p}, u_{t1n} and\ u_{t10}$ are positive, negative, and zero-sequence components of fundamental frequency and $u_{t\square}$ is the harmonic component of the bus voltage.

As per the control objectives of the MCUPQC, the amplitude of the load voltage should be kept as a constant sinusoidal wave even though the bus voltage is disturbed. Therefore, the expected load voltage in the synchronous reference frame ($u_{l\_dqo}^{exp}$) has only one value

$$u_{l\_dqo}^{exp} = T_{abc}^{dqo} u_{l\_abc}^{exp} = \begin{bmatrix} U_m \\ 0 \\ 0 \end{bmatrix} \quad (13)$$

where the load voltage in the abc reference frame ($u_{l\_abc}^{exp}$) is

$$u_{l\_abc}^{exp} = \begin{bmatrix} U_m \cos(\omega t) \\ U_m \cos(\omega t - 120^0) \\ U_m \cos(\omega t + 120^0) \end{bmatrix} \quad (14)$$

The compensating reference voltage in the synchronous dq0 reference frame is defined as below

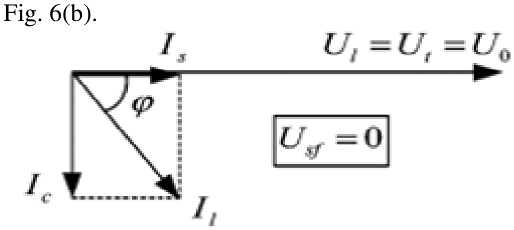
$$u_{sf\_dqo}^{ref} = u_{t\_dqo} - u_{l\_dqo}^{exp} \quad (15)$$

This means that in (12) voltage should be maintained constant all other unwanted \ components must be eliminated. The compensating reference voltage in (15) is then transformed back into the abc reference frame, the output compensation voltage of the series VSC can be obtained by Implementing an improved SPWM voltage control technique. Christo Ananth et al.[4] discussed about E-plane and H-plane patterns which forms the basis of Microwave Engineering principles.

POWER-RATINGANALYSIS OFTHE MCUPQC

Coming to the cost concern the power rating of the MCUPQC is an important factor before calculating .

Fig. 6 represents the phasor diagram of this scheme with and without voltage sag condition under a typical load power factor. The series-injected voltage becomes zero when the bus voltage is at the desired value [Fig. 6(a)]. reactive component of load current is injected by shunt VSC that For the sag compensation in this model, the quadrature series voltage injection at the desired value of bus voltage is needed as shown in Fig. 6(b).



(a)

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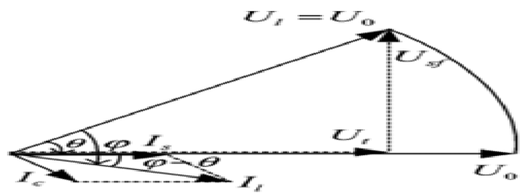

(b)

Fig. 6. Phasor diagram of quadrature compensation. (a) Without voltage sag. (b) With voltage sag

The phasor diagram of Fig. 7 explains the operation of this scheme in case of a voltage sag.

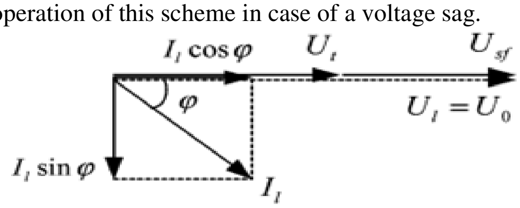

Fig. 7. Phase diagram of in phase compensation

A comparison between in phase (UPQC-P) and quadrature models is made for different sag conditions and load power factors in [13]. In the UPQCQ model the power rating of the shunt VSC model is lower than that of the UPQCP and in the UPQC-P model the power rating of the series-VSC is lower than that of the UPQC-Q for the power factor less than equal to 0.9.Also, it is observed that the total power rating of UPQCQ model is lower than that of UPQC-P model where the VAR demand of the load is high.

As explained in Section B, the power needed for interruption compensation in Feeder2 must be supplied through the shunt VSC in Feeder1 and the series VSC in Feeder2. This means that power ratings of these VSCs are greater than that of the series VSC in Feeder1.

Based on the fore mentioned discussion, the power-rating calculation for the MC-UPQC is carried out on the basis of the linear load at the fundamental frequency. The parameters in Fig. 6 are corrected by adding suffix "1," indicating Feeder1, and the parameters in Fig. 7 are corrected by adding suffix "2," indicatingFeeder2. As shown in Figs. 6 and 7, load voltages in both feeders are kept constant at regardless of bus voltages variation, and the load currents in both feeders are assumed to be constant at their rated values

$$U_{l1} = U_{l2} = U_0 \quad (16)$$

$$\begin{cases} I_{l1} = I_{01} \\ I_{l2} = I_{02} \end{cases} \quad (17)$$

.

The voltage injected by the series VSC in Feeder1 can be written as in (22) from fig(6) and hence the power rating of this converter Calculated

$$U_{sf1} = U_{t1} \tan\theta = U_0(1 - x_1) \tan\theta \quad (18)\ c$$

$$S_{VSC1} = 3U_{sf1}I_{s1} = 3U_0(1 - x_1)\tan\theta * \left(\frac{I_{01}\cos\varphi_1}{1-x_1} + \frac{x_2 I_{02}\cos\varphi_1}{1-x_1}\right) \quad (19)$$

The shunt VSC current is divided into two parts.

1) The first part (i.e., I_{c1}) compensates for the reactive component of Feeder1 current and can be calculated from Fig. 6 as

$$I_{c1} = \sqrt{I_{l1}^2 + I_{s1}^2 - 2I_{l1}I_{s1}\cos(\varphi_1 - \theta)}$$
$$= \sqrt{I_{01}^2 + I_{s1}^2 - 2I_{01}I_{s1}\cos(\varphi_1 - \theta)} \quad (20)$$

This I_{c1} of the shunt VSC only exchanges reactive power (Q) with the system.

2) The second part shunt VSC current provides the real power (P) that is needed for sag or interruption compensation inFeeder2. The power rating calculation of the shunt VSC is as below,

$$S_{VSC2} = 3U_{l1}I_{pf} = 3\sqrt{Q^2 + P^2}$$
$$= 3\sqrt{(U_{l1}I_{c1})^2 + (U_{sf2}I_{l2}\cos\varphi_2)^2}$$
$$= 3U_0\sqrt{I_{c1}^2 + (x_2 I_{02}\cos\varphi_2)^2} \quad (21)$$

Therefore the power rating of the series-VSC in Feeder2 is calculated by (20). Under the worst-case (like, interruption compensation) conditions, one must consider $x_2 = 1$ and then

$$S_{VSC3} = 3U_{sf2}I_{l2} = 3x_2U_0I_{02} \quad (22)$$

SIMULATION RESULTS

The proposed MCUPQC and its control schemes have been tested through extensive case study simulations using MATLAB (SIMULINK). In this section, the performance of the proposed MCUPQC system is shown through simulation results.

A. Distortion and Sag/Swell on the Bus Voltage

Let us consider that the power system in Fig. 2 consists of two three-phase three-wire 380(v) (rms,L-L), 50Hz utilities. The BUS1 voltage contains the seventh-order harmonic with a value of 22%, the BUS2voltage contains the fifth order harmonic with a valueof35%. The BUS1 voltage contains 25% sag between 0.1s < t < 0.2s and 20% swell between 0.2 s < t < 0.3s. TheBUS2 voltage contains 35% sag between 0.15s < t < 0.25s and 30% swell between 0.25s < t < 0.3s. The nonlinear/sensitive load L1 is a three phase rectifier load which supplies an RC load of 10and30 F. Finally, the critical load L2 contains a balanced RL load of 10and 100 mH.

The MCUPQC is switched-on at t= 0.02 s. The BUS1 voltage, the corresponding compensation voltage injected by VSC1, and finally load L1voltage are shown in Fig.8. In all figures, only the phase wave form is shown for simplicity.

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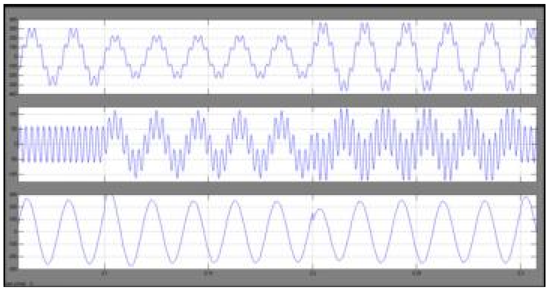

Fig. 8. BUS1 voltage, series compensating voltage, and load voltage in Feeder1.

BUS1 and BUS2 are satisfactorily compensated with a good dynamic response. The nonlinear load current generated by the load1 is compensated by injecting corresponding compensating current by VSC2. Compensated Feeder1 current the dc link capacitor voltages are shown in Fig.10. The distorted nonlinear load current is compensated very well and the total harmonic distortion (THD) of the feeder current is brought to below5% from 28.5%. Also, the dc voltage regulation loop functioned properly under all disturbance test conditions, such as sag/swell in both the feeders.

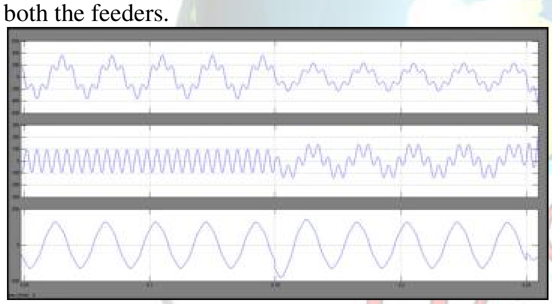

Fig. 9. BUS2voltage, series compensating voltage, and load voltage inFeeder2.

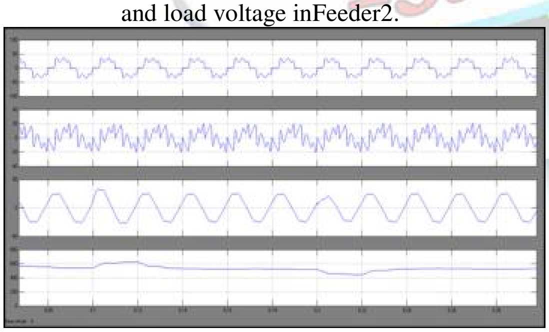

Fig. 10. Nonlinear load current compensating current, Feeder1 current, and capacitor voltage.

B. Up stream Fault on Feeder2

When a fault occurs in Feeder2 the voltage across the sensitive/critical load L2 is involved in sag/swell or interruption. This voltage imperfection will be compensated by VSC2. In this case, the power demand by load L2 is suppliedbyVSC2 and VSC3. This implies that the power semiconductor switching devices ofVC2 and VSC3 are rated such that total power transfer is possible.

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Therefore the cost of the MCUPQC must be balanced against the cost of interruption, based on reliability indices, such as the customer average interruption duration index interruption frequency index. It may be expected that the installation cost of MCUPQC can be recovered within few years by charging higher tariffs on the protected lines. By applying a three-phase to ground fault on Feeder2 between 0.3s<t<0.4s, the performance of the MCUPQC is tested. Simulation results are shown in Fig. 11.

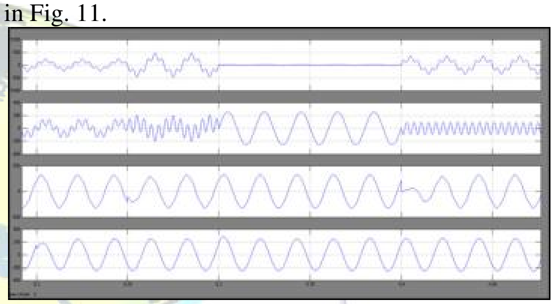

Fig. 11. Simulation results for an upstream on Feeder2: BUS2 voltage, compensating voltage, and loads L1 and L2 voltages.

C. Load Change

To evaluate the system behavior during a load change, the nonlinear load L1 is doubled by reducing its resistance to half at 0.5 s. The other load, however, is kept unchanged. The system response is shown in Fig. 12. It is observed that as load L1 changes, the load voltages offeeder2 remains undisturbed, the dc-link capacitor voltage is regulated and the nonlinear load current is compensated.

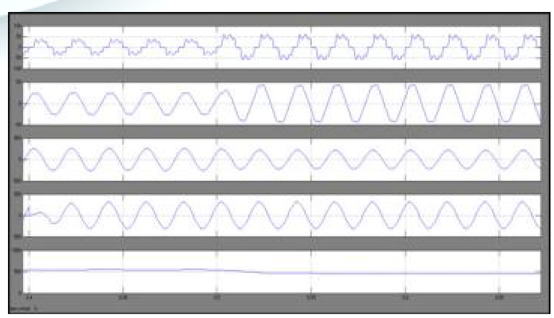

Fig. 12. Simulation results for load change: nonlinear load current, Feeder1current, load L1 voltage, load L2 voltage, and dc link capacitor voltage.

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D. Unbalance Voltage

The control strategies for shunt and series VSCs are based on the dq method. They are capable of compensating unbalanced source voltage and unbalanced load current. To evaluate the control system capability under unbalanced voltage conditions, a new simulation is to be performed. In this simulation, the BUS2voltageand the voltage harmonic components ofBUS1 are similar to those given in Simulation results. However, the fundamental component of voltage in the BUS1 is unbalanced three phase voltage with an unbalance factor of 40%. Such an unbalance voltage is given by

$$U_{t1,fundamental} \begin{bmatrix} 0.31\cos(\omega t + 46^0) \\ 0.31\cos(\omega t - 106^0) \\ 0.155\cos(\omega t - 210^0) \end{bmatrix} \quad (23)$$

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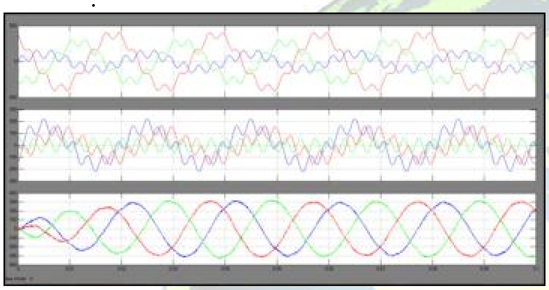

Fig. 13. BUS1 voltage, series compensating voltage, and load voltage in Feeder1 under unbalanced source voltage.

CONCLUSION

In this project we are implementing configuration for the simultaneous compensation of the current and voltage in two individual feeders that has been proposed. The new configuration which is named as the multi converter unified power quality conditioner (MCUPQC). When compared with the conventional UPQ, the proposed topology has the capability of protecting the critical and sensitive loads against the distortions, sags/swell, and interruption in two-feeder systems. This can be extended to multi bus/ multi feeder systems by adding more series and shunt VSCs depending on the load conditions. The performance of the MCUPQC is analyzed under various disturbance conditions and it is shown that the proposed MC-UQC offers the following advantages: 1) sharing power compensation capabilities between two adjacent feeders that are not connected; 2) supports power transfer between two adjacent feeders during sag/swell and interruption compensation on one feeder; 3) Provides compensation for interruptions without battery storage system and consequently without storage capacity limitation.

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