ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Issue 7, July 2017

OPTIMIZED LLR-2^K b SCL DECODER FOR POLAR CODES

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Abstract-Because of their ability accomplishing property, polar codes have turned out to be a standout amongst the most appealing channel codes. To date, the progressive cancelation list (SCL) unraveling calculation is the essential approach that can ensure extraordinary mistake revising execution of polar codes. Nonetheless, the equipment outlines of the first SCL decoder have huge silicon territory and long unraveling idleness. Although some current endeavors can diminish either the territory or idleness of SCL decoders, these two measurements still can't be advanced in meantime. This paper, interestingly, proposes a general log-probability proportion (LLR)-based SCL disentangling calculation with multi-bit choice. This new calculation, alluded as LLR-2^Kb-SCL, can decide 2^K bits at the same time for subjective K with the utilization of LLR messages. What's more, a diminished information width plot is displayed to decrease the basic way of the arranging piece. At that point, in view of the proposed calculation, a VLSI engineering of the new SCL decoder is produced., the proposed LLR-2^Kb-SCL decoders accomplish noteworthy decrease in both zone and dormancy when contrasted with earlier works. Subsequently, And also this paper shows performance of the LLR-2^Kb-SCL to be improved by modifing the MCU block.

IndexTerms— polarcodes, successive-cancellation,VLSI, log-likelihood-ratio (LLR), multi-bit decision, PASTA.

I.INTRODUCTION

POLAR codes are one of the most attractive Forward Error Correction (FEC) codes.This codes having unique capacity-achieving property[1], so polar codes provide outstanding error-correcting capability that would be very useful for digital transmission. But dealing with polar codes, they suffer from inferior finite length error-correcting performance. In the region of short or medium code length, polar codes are not comparable to the LDPC codes in terms of coding gain. So for that successive-cancellation list (SCL) decoding algorithm was proposed to improve the coding gain of the polar codes[2]. The SCL algorithm for polar codes can outperform the WiMAX LDPC codes even for a shorter code-length, and also it can help for polar codes achieve beyond-LDPC performance,but this approach suffers from high complexity and long latency[3]. To solve this problems recently some efforts were proposed. An LLR-based SCL algorithm was proposed by B.Yuan[4] to reduce the amount of combinational logic and memory. In low-latency SCL algorithms were presented to reduce the required number of decoding cycles[5]. However, these prior works

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ISSN 2394-3785 (Online)
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Vol. 4, Issue 7, July 2017

only focused on either reducing area or latency, but not on optimizing these two metrics at the same time.

POLAR CODES

Polar codes are discoversed by Erdal Arıkan in 2009 and they provide the first deterministic construction of capacity-achieving codes for binary memory less symmetric (BMS) channels [1].

In particular, consider a setup where (U1, U2) are two equiprobable bits that are encoded into (X1, X2) = (U1 ⊕ U2, U2). Then, (X1, X2) are mapped to (Y1, Y2) by two independent BMS channels with transition probabilities P(Y1 = y | X1 = x) = P(Y2 = y | X2 = x) = W(y|x). The factor graph for this setup is shown in Fig.1. Since the mapping from (U1, U2) to (X1, X2) is invertible, one finds that

I(U1, U2; Y1, Y2) = I(X1, X2; Y1, Y2) = I(X1; Y1) + I(X2; Y2) = 2I(W),

where C=I(X1; Y1) = I(W) is the capacity of symmetric BMS channel because X1 is equiprobable and

$$I(W) \triangleq \sum_y W(y|0)\, log_2[W(y|0)\,/(\tfrac{1}{2}W(y|0)+(\tfrac{1}{2}W(y|1))]=I[X_1;Y] \quad (1)$$

Thus, the transformation (X1,X2)=(U1⊕U2,U2) preserves the sum capacity of the system. Also, the chain rule decomposition I(U1, U2; Y1, Y2) = I(U1; Y1, Y2) + I(U2; Y1, Y2|U1) = 2I(W).Implies that one can also achieve the rate 2I(W) using two steps. First, information is transmitted through the virtual channel W− : U1→(Y1, Y2) at a rate I(U1; Y1, Y2) and decoded to $\hat{u}_1$. Then, data is transmitted through the virtual channel W+ : U2 → (Y1, Y2, U1) at a rate I(U2; Y1, Y2|U1) and decoded to $\hat{u}_2$ based on the side information $\hat{u}_1$.

If one uses convolution codes with sequential decoding, however, the expected decoding complexity per bit becomes unbounded for rates above the computational cutoff rate.

$$R0(W) = 1 - \log_2(1 + Z(W)),$$

Where $Z(W) = \sum_y \sqrt{W(y|0)W(y|1)}$ is the Bhattacharyya parameter of the channel. Arıkan's key observation was that, while the sum capacity of the two virtual channels is preserved, the sum cutoff rate satisfies the below condition.

$$R0(W+) + R0(W-) \geq 2R0(W),$$

with equality if R0(W) ∈ {0, 1}. Thus, repeated transformations of this type cause the implied virtual channels to polarize into external channels whose capacities approach 0 or 1. But, for these external channels, coding is trivial and one either sends an information bit or a dummy bit. From a theoretical point of view, polar codes are beautifully simple. Practically, they approach capacity rather slowly as their block length increases and, thus, are not yet competitive with good photograph LDPC codes for moderate block lengths.

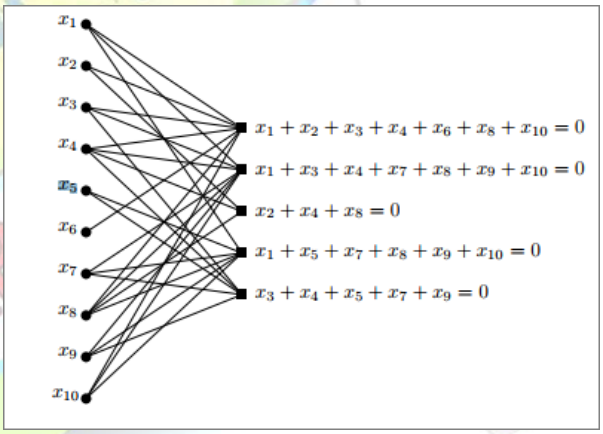

Figure 1: An LDPC code

II. REVIEW OF POLAR CODES

A. Encoding of Polar Codes

The encoding procedure of (n, p) polar codes consists of two steps. First, the p-bit source message is extended to an n-bit message u=(u1, u2,…un) with padding n-p "0" bits. Here those padded "0" bits are referred as frozen bits and their positions over the u, namely frozen positions, are known to both the transmitter and

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
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International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Issue 7, July 2017

sreceiver. Then, u is multiplied with an n-by-n generator matrix G to obtain the transmitted codeword x=(x1, x2,…,xn)=uG. Fig. 1 shows the example of an n=4 polar codes encoder. For details on encoding of polar codes, the reader is referred to [1].

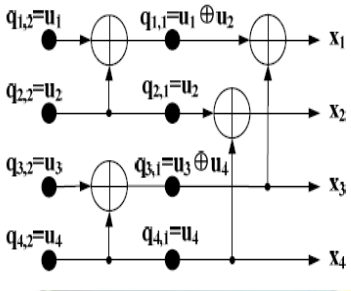

Fig.2. n=4 polar encoder

B.Successive-Cancellation(SC)Decoding Algorithm

SCL decoding algorithm is proposed to enhance the performance of SC decoding for short and moderate block lengths in [4].SCL decoding enables tracking L best decoding paths concurrently, unlike an SC decoder can track at most a single decoding path. If L is sufficiently large, ML decoding performance is achieved, since sufficient number of decoding paths are visited. There is a trade-off between complexity and performance of the algorithm, because time complexity (Y_{SCLD}) and space complexity (ζ_{SCLD}) of the algorithm linearly depends on list size (L) such that

$$\gamma_{SCLD}(L,N) = O(L,N\ logN)$$

$$\zeta_{SCLD}(L,N) = O(L,N) \qquad (2)$$

A high level description of the algorithm is shown in Fig.3. The SCL algorithm takes the received code word y_1^N , the code block length N, the information set A, the frozen bit vector u_{A^c} and the maximum list size L as input and calculates the estimated information bits $\hat{u}_A$ as output. The current list size variable, cL set as 1 at the initialization of the algorithm.

Algorithm 2: Successive Cancellation List Decoding

Input: received codeword, y_1^N
Input: code block length, N
Input: information set, $\mathcal{A}$
Input: frozen bit vector, $u_{\mathcal{A}^c}$
Input: maximum list size, L
Output: estimated information bits, $\hat{u}_{\mathcal{A}}$
Variable: $cL \leftarrow 1$ `//current list size`

```
1  begin
2    for i ← 1 to N do
3      if i ∉ A then
4        for l ← 1 to cL do
5          û_{l,i} ← u_i
6      else
7        if cL ≠ L then
8          for l ← 1 to cL do
9            û_{l,i} ← 0
10           û_{l+cL,i} ← 1
11         cL ← 2cL
12       else
13         s ← sort (W_N^(θ)(y_1^N, û_1^{i-1} | û_{1,i}^L))
14         for l ← 1 to cL do
15           û_{l,i} ← s_l
16   return û_A
```

Fig.3 SCL decoding algorithm

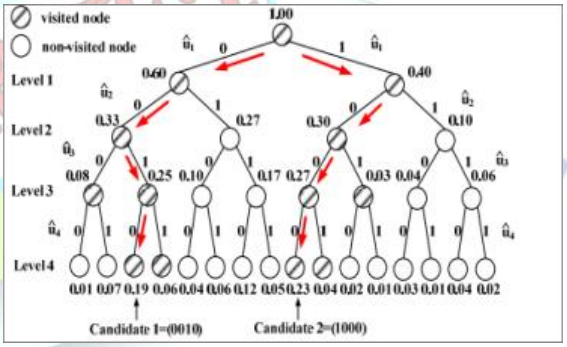

Fig. 4. Searching of SCL decoder

III.THE PROPOSED LLR-BASED MULTI-BIT DECODING

From Fig.4.it can be seen that the SCL calculation needs to visit the hubs at each level of the code tree. This navigating looking style prompts a long deciphering inactivity. To address this issue, a decreased inactivity calculation that can decide 2^K bits. Be that as it may, the approach

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Issue 7, July 2017

depends on the probability messages, which requires substantially bigger calculation and memory unpredictability than the ordinarily utilized LLR-based decoder. Then again, those LLR-based SCL decoders are just ready to decide one piece in one cycle; henceforth they have any longer dormancy than the decoder. Thus, to date those earlier SCL decoders are not ready to lessen the dormancy and range in the meantime. [9] discussed about Improved Particle Swarm Optimization. The fuzzy filter based on particle swarm optimization is used to remove the high density image impulse noise, which occur during the transmission, data acquisition and processing. The proposed system has a fuzzy filter which has the parallel fuzzy inference mechanism, fuzzy mean process, and a fuzzy composition process. In particular, by using no-reference Q metric, the particle swarm optimization learning is sufficient to optimize the parameter necessitated by the particle swarm optimization based fuzzy filter, therefore the proposed fuzzy filter can cope with particle situation where the assumption of existence of "ground-truth" reference does not hold. The merging of the particle swarm optimization with the fuzzy filter helps to build an auto tuning mechanism for the fuzzy filter without any prior knowledge regarding the noise and the true image. Thus the reference measures are not need for removing the noise and in restoring the image. The final output image (Restored image) confirm that the fuzzy filter based on particle swarm optimization attain the excellent quality of restored images in term of peak signal-to-noise ratio, mean absolute error and mean square error even when the noise rate is above 0.5 and without having any reference measures.

A. LLR-based Multi-bit SCL Decoding

This subsection introduces a LLR-based SCL unraveling calculation with 2^K bits choice, in particular LLR-2^Kb-SCL. Notice additionally proposed a decreased dormancy decoder that can decide various bits in one cycle. Be that as it may, the SCL decoder depends on the probability frame while the plan in this paper depends on the LLR shape. This distinction in the principal portrayal of the proposed calculation prompts considerably less calculation many-sided quality. Next, we demonstrate to decide each progressive 2^K bits as $u_{2^k}(i-1)+1 \dots \dots u_{2^k} i$ at a similar time in the LLR shape. From the perspective of code tree (see Fig. 4), this implies the SCL decoder can straightforwardly compute the measurements of length-(2^Ki) ways from the measurements of length-(2^K(i-1)) ways. All in all, such direct calculation is performed by a LLR-based metric calculation unit (MCU), which replaces the first last K phases of each LLR-based SC decoder (see Fig. 3). In the accompanying passage, we demonstrate to infer the capacity of the LLR-based MCU. Expect that the beforehand decoded 2^K(i-1) bits u2^K(i-1) are z1...z2^K (i-1) individually. This occasion is indicated as $u_1 2^K$(i-1). In this way, in the logarithmic space the length-(2^Ki) way metric can be spoken to as:

$$M\left(\alpha_1 \dots \alpha_{2^k}, z_1^{2^k(i-1)}\right) \triangleq ln\left(pr(\hat{u}_{2^{k(i-1)}+1}^{2^i} = \alpha_1^{2^k(i-1)} u1 = z_1^{2^k(i-1)})\right) \quad (3)$$

that is the set of the current 2^K decoded bits.In addition,$\propto_1^{2^k}$is defined as$\propto \cdots \propto_1^{2^k}$whose elements are the binary values. Eqn(3) contains the probabilistic data of the current 2^K decoded bits, which is obscure amid the translating system. To address this issue, we have to additionally speak to the logarithmic way measurements with the LLR messages that are input to the MCU. Such reformulation depends on the way that the polar

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
Available online at www.ijartet.com

International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Issue 7, July 2017

translating methodology is inalienably "guided" by its encoding strategy. Synchronous appropriate to-left translating methodology of the progressive 2^K bits (see Fig. 5(a)) includes the estimation of the left-to-right encoding system (see Fig. 5(b)).

$$M\left(\alpha_1 \dots \alpha_{2^k}, z_1^{2^{k(i-1)}}\right) \triangleq ln\left(pr(\widehat{out}_1^{2^k} = \alpha_1^{2^k} U, \hat{u}_1^{2^{k(i-1)}} = z_1^{2^{k(i-1)}})\right) \quad (4)$$

Notice that the determination of $\widehat{out_1}$,…, $\widehat{out}_{2^k}$ are independent. In addition, if we denote the *j*-th column vector of $\boldsymbol{U}$ as $\boldsymbol{U}(j)$, then we have $\widehat{out} = \propto_1^{2^k} U(j)$.

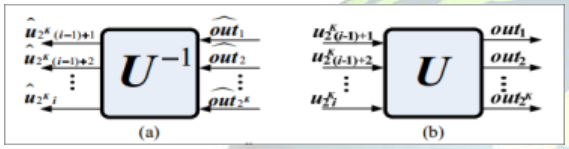

Fig. 5. (a) right-to-left decoding of 2^K bits. (b) left-to-right encoding bits.

As a result, Eqn(4) can be further derived as below:

$$M\left(\alpha_1 \dots \alpha_{2^k}, z_1^{2^{k(i-1)}}\right) = ln\left(pr(\widehat{out}_1^{2^k} = \alpha_1^{2^k} U / \hat{u}_1^{2^{k(i-1)}} = z_1^{2^{k(i-1)}}) pr(u_1^{2^{k(i-1)}} = z_1^{2^{k(i-1)}})\right)$$
$$= \sum_{j=1}^{2^k} ln\left(pr(\widehat{out}_j = \alpha_1^{2^k} U(j) / \hat{u}_1^{2^{k(i-1)}} = z_1^{2^{k(i-1)}})\right) + M(z_1^{2^{k(i-1)}}) \quad (5)$$

Recall that each SC component decoder is based on LLR form. In that case, the *j*-th input to the MCU block is:

$$S_j = \ln \frac{\Pr\left(\widehat{out}_j = 0 | u_1^{2^{k(i-1)}} = z_1^{2^{k(i-1)}}\right)}{\Pr\left(\widehat{out}_j = 1 | u_1^{2^{k(i-1)}} = z_1^{2^{k(i-1)}}\right)} \quad (6)$$

As a result, we can obtain the elements of t first item in Eqn(5):

$$\Pr\left(\widehat{out}_j = 0 | \hat{u}_1^{2^{k(i-1)}} = z_1^{2^{k(i-1)}} \frac{e^{s_j}}{e^{s_j}+1}\right) ,$$

$$\Pr\left(\widehat{out}_j = 1 | \hat{u}_1^{2^{k(i-1)}} = z_1^{2^{k(i-1)}} \frac{e^{s_j}}{e^{s_j}+1}\right) \quad (7)$$

Substituting Eqn(7) into Eqn(5), we have:

$$M\left(\alpha_1 \dots \alpha_{2^k}, z_1^{2^{k(i-1)}}\right) = \sum_{j=1}^{2^k} (s_j \left(1 - \alpha_1^{2^k} U(j)\right) - ln(e^{s_j} + 1)) + M(z_1^{2^{k(i-1)}}) \quad (8)$$

Eqn (8) depicts the LLR-based refresh guideline for way measurements. Once the MCU square gets the 2^K input LLR messages s_j and the past metric of length-(2^K(i-1)) way, it can promptly compute the new metric of length-(2^Ki) way with the utilization of (8), which compares to the concurrent choice for 2^K bits. Notice that (8) contains exponential and logarithmic capacities, which require long basic ways in equipment plan. Along these lines, (8) should be improved for possible VLSI execution.

Consider ln(1+*ex*)≈*x* for large *x*; otherwise 0 for small *x*. Eqn(8) can be further approximated as below:

$$M\left(\alpha_1 \dots \alpha_{2^k}, z_1^{2^{k(i-1)}}\right) = \sum_{j=1}^{2^k} (s_j \left(1 - \alpha_1^{2^k} U(j)\right) - \delta(s_j)) + M(z_1^{2^{k(i-1)}}) \quad (9)$$

Eqn(9) demonstrates to specifically compute the metric of length-(2^Ki) ways from the metric of length-(2^K(i-1)) ways. With the utilization of this refresh standard, we can build up the LLR-based SCL unraveling calculation with 2^K bits choice as Scheme-A. All in all, a L-estimate LLR-2^Kb-SCL decoder comprises of L duplicates of LLR-based SC decoder. To translate each 2^K progressive bits, every SC segment decoder initially plays out the general SC unraveling methodology till the last-(m-K) arrange (see Fig. 4), where m=$\log_2$n. Right now, the (m-K) organize yields 2^K LLR messages s_j (j=1, 2,… 2^K) to the MCU piece. At that point, the MCU obstruct in every SC part decoder computes the new way measurements with the utilization of eqn(9). From that point forward, the majority of the refreshed way measurements from the L SC segment decoders are looked at and L biggest are chosen as the survival ways measurements. The above whole technique is rehashed for each 2^K bits until the point when all the n bits are resolved. Note that like [5], a straightforward zero-compelling unit (ZFU) is required after the calculation of (9), which drops the inadequate ways that damage the solidified conditions.

ISSN 2394-3777 (Print)
ISSN 2394-3785 (Online)
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International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Issue 7, July 2017

B. Lessened Data-Width Scheme for Sorting Block

Regularly, Q=6 bit quantization plot is adequate for the settled point usage of LLR-based SCL decoder. In any case, as demonstrated in [3], the portrayal of way measurements needs more bits since the way measurements have bigger information run than the engendered LLR messages. In [3], it demonstrated that M=8 bit for way measurements can keep away from critical execution corruption regarding outline mistake rate (FER).Since the general basic way of the SCL decoder is in the arranging hinder that sorts those way measurements [3][5], the heightening information width of way measurements unavoidably causes huge increment in basic way delay. To address this test, we propose a decreased piece width conspire for arranging square. The key thought is to just use S=M-1 bits to speak to the way measurements for arranging, while the portrayals of way measurements for refreshing and putting away are as yet in view of M bits. This approach is gotten from the accompanying perception. In SCL decoder the arranging square does not require as high accuracy as MCUs, since the capacity of the sorting piece is simply to rank the way measurements without changing their esteems, while the MCUs need to receive bigger information width to ensure precise figuring. In this way, a diminished information width for arranging piece does not cause noteworthy execution debasement but rather empowers lessening in basic way delay.

Fig. 6shows the settled point reenactment comes about for the proposed LLR-2^Kb-SCL calculation with diminished information with for arranging piece. Here the reenactment condition is AWGN channel with BPSK balance and the code parameters are n=1024, r=0.5. From the figure it can be seen that, contrasted with the first plan utilizing S=8 bits for arranging the way metric, the proposed conspire with S=7 bits just has insignificant execution misfortune for various estimations of K and L.

HARDWARE ARCHITECTURE

A. Overall Architecture

Fig. 6 demonstrates the general equipment design of the proposed L-estimate LLR-2^Kb-SCL calculation decoder. The information way of the whole decoder contains L number of LLR-based SC decoders in addition to a metric arranging piece. For every SC part decoder, it is reformulated from the LLR-based decoder in [8], which holds the (m-K) arranges however the last K stages are supplanted by the LLR-based MCU and ZFU. Also, the required memory asset of the whole decoder comprises of enlist clusters, mass memory and cradle for survival ways, way measurements, proliferating LLR messages and channel yields, individually. In this segment, the equipment plan of the arranging square is exceptionally direct .

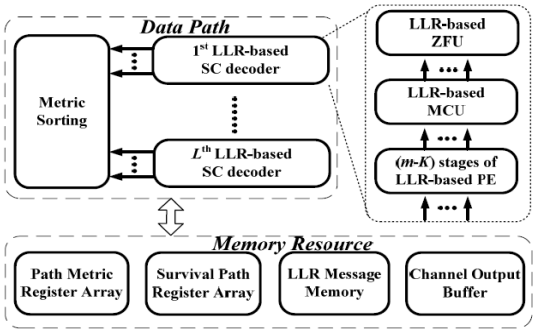

Fig.6. Overall architecture of the LLR-2^Kb-SCL decoder

B.LLR-based Metric Computation Unit (MCU)

Section III portrays the capacity of MCU. Since this capacity relies upon K, the equipment plan of MCU shifts with various decisions of K. Fig. 7 outlines the inward engineering of MCU for

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ISSN 2394-3785 (Online)
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K= 3. Here δ(•) piece can be basically actualized with a multiplexer. What's more, StoC and CtoS pieces speak to the parts that play out the change between sign-extent and 2's supplement shapes.

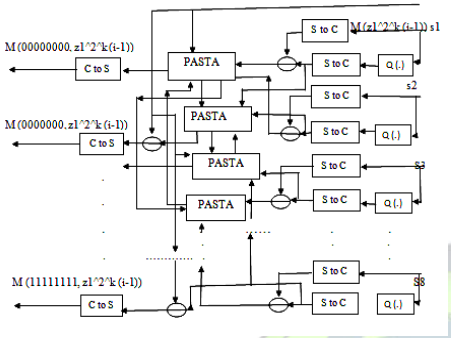

Fig.7.Modified MCU

The above Fig.7.is modified MCU that we seen in [5] normally MCU having more number of XOR gate that means those are half adders, because of them latency and complexity is more. To reduce that all the adders are replaced by parallel self timed adder (PASTA).

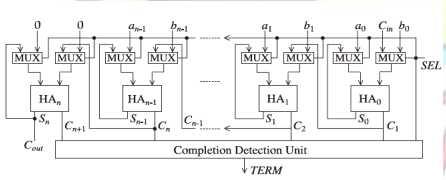

Fig. 8.PASTA architecture

The below Fig.8.shows the diagram of parallel self timed adder, It is based on a recursive formulation for performing multi bit binary addition[11]. The design of PASTA is regular and uses half-adders (HAs) along with multiplexers requiring minimal interconnections. Thus, it is suitable for VLSI implementation. The design works in a parallel manner for independent carry chain blocks. The selection input for two-input multiplexers corresponds to the Req handshake signal and will be a single 0 to 1 transition denoted by SEL. It will initially select the actual operands during SEL = 0 and will switch to feedback/carry paths for subsequent iterations using SEL = 1. The feedback path from the HAs enables the multiple iterations to continue until the completion when all carry signals will assume zero values.

IV. SIMULATION RESULT

The simulation results of the LLR-2^Kb SCL decoder and LLR-2^Kb SCL with PASTA are shown in Fig.9. and Fig.10.

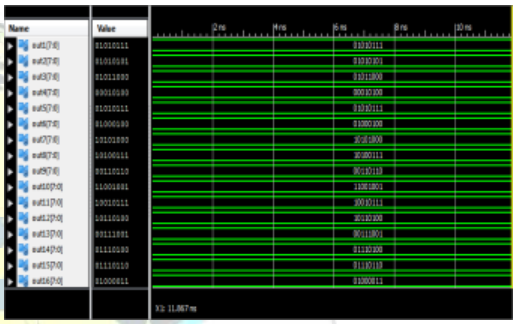

Fig.9.Output wave forms of LLR-2^Kb SCL decoder

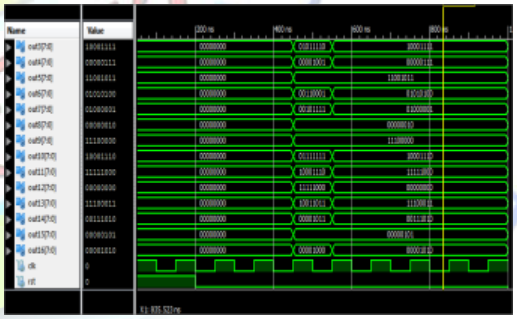

Fig.10.Output wave forms of LLR-2^Kb SCL with PASTA

These two decoders are synthesized under the constraint of 400MHz in Xilinx ISE 13.2 targeting for Virtex-6 XC6VSX315T device FF1156 package with a speed grade of -3.

Comparisons between proposed and extended designs:

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ISSN 2394-3785 (Online)
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International Journal of Advanced Research Trends in Engineering and Technology (IJARTET)
Vol. 4, Issue 7, July 2017

Parameters	LLR 2^Kb SCL decoder	LLR 2^Kb SCL decoder with PASTA
Latency	6.183ns	4.745ns
Memory used	1335MB	933MB
Power	4.447mW	4.262mW
Frequency	161.22MHZ	210.74MHZ

V. CONCLUS ION

This paper is about design and implementation of LLR-2^Kb-SCL decoder for polarcodes. The experimental results show that the proposed LLR 2^Kb SCL decoder with PASTA is compared with LLR-2^Kb-SCLdecoder can reduce the latency by 76.7%, and memory usage reduced by 69.8%, so that complexity also reduces at the same time without loss in the performance of the polar decoder.

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