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A Modified Parallel Prefix CI-CSK Adder

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Abstract*—In this paper we present a modified carry skip adder structure by replacing some of the middle stages of CI CSK by parallel prefix The concatenation and incrementation technique is used for speed and efficiency.By using the parallel prefix structure we can achieve more faster and efficient CSKA.The advantage of this structure is that reduces the number of stages ,delays and the slack time. Prefix network is done by using the Brent kung adder which have lowest fan out. using the parallel prefix structure we can generate carry fastly.High speed and energy efficient carry skip can be obtained by using this modified parallel prefix CI-CSK adder.*

Keywords—Carry skip adder(CSKA),Concatenation and Incrementation(CI-CSK),Parallel Prefix Adder(PPA)

I. INTRODUCTION

Addition is one of the most important arithmetic operation in a digital system.[1] In order to perform the addition we need an efficient adder.Efficient adder in terms of speed,power,and energy.different type of adder families are there like ripple carry adder(RCA),Carry select adder(CSLA),Carry lookahead adder,carry skip adder etc.in this carry skip adder(CSKA) is an efficient adder considering both delay and energy[2].

Carry skip adder[3] means which can skip the carry when group of full adders are in propagate mode.The output carry of a particular stage will be equal to input carry when the group of full adders in that particular stage is in propagate mode.In conventional CSKA the skip logics is perform by multiplexer.the disadvantage of conventional structure is that its delay and area is more.because the multiplexer needs 12 transistors and crtical path delay consists of all RCA blocks and multiplexer logic.

The modified parallel prefix CI-CSK adder consist of the following.by combining the incrementation and concatenation technique we can made an efficient adder.The concatenation technique is used for the speed enhancement and the incrementation technique is done for efficiency.In CI-CSKA the skip logic is perform by AOI/OAI gates.The peculiarity of AOI/OAI gate is that it consists only fewer transistors,lower delay,area and power.

Parallel prefix adder (PPA) structure is one of the fastest adder structure.By combining PPA to CICSKA we get fastest carry skip adder.There are different types of PPA are there.Brent kung adder is used in this modified structure.The merits of brent kung adder is that it have lower fan out and wiring delays.

Parallel Prefix Adders are also known as carry lookahead adders.PPA mainly consists of three stages.The first stage is called preprocessing,second stage is called carry generation and third stage is called post processing.The post processing stage gives the output sum result.

The rest of the section is organized as follows.Section II discuss about conventional carry skip adder,Section III discuss about AOI/OAI skip logic,section IV discuss about modified parallel prefix adder ,section V discuss about simulation results and finally section VI gives the conclusion.

II. MULTIPLEXER SKIP LOGIC

The Multiplexer skip logic is consider as conventional carry skip adder. It consists of RCA blocks, multiplexer and basic logic gates.The multiplexer is used as the skip logic.The basic logic gates used are AND and XOR gates.XOR gate check whether the input bit are different or not.The output of XOR gates are given to AND gate .The AND gate is used as the selector signal for MUX.The MUX select the output according to the selector signal.If the signal is one MUX select the previous carry and otherwise it select the generated carry.The disadvantage of the structure is that critical path delay and skip logic area is more.

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III. AOI/OAI CI-CSK ADDER

The disadvantageous of conventional skip adder is overcome by AOI/OAI CI-CSK adder.Three changes are made to conventional carry skip adder.Multiplexer skip logic is replaced by AOI/OAI logic gate and also added concatenation and incrementation techniques.Concatenation technique means except the first RCA block all the other block have an input carry as zero.so.the RCA block can process their operation simultaneiously.The RCA block doesnot need to wait for the previous carry for their operation. The output of RCA block is called intermediate results. the inputs to incrementation block are intermediate results and previous carry and produces the output sum.the skip logic is perform by AOI/OAI gate. It consists only less number of transistors, less delay and area.it is a easy logic.The skip logic needs only six transistors. The concatenation block is used for speed and incrementation block is used for efficiency.the inputs to skip logic are output from RCA block, intermediate results products and previous carry.if the output of RCA block is one the output of skip logic is equal to output of RCA block. If the output of RCA block is zero the output of skip logic depends on output of intermediate results and previous carry.so here the propagation delay and critical path delay is less. This structure is more energy efficient than conventional structure. [4] proposed a system in which the complex parallelism technique is used to involve the processing of Substitution Byte, Shift Row, Mix Column and Add Round Key. Using S-Box complex parallelism, the original text is converted into cipher text. From that, we have achieved a 96% energy efficiency in Complex Parallelism Encryption technique and recovering the delay 232 ns. The complex parallelism that merge with parallel mix column and the one task one processor techniques are used. In future, Complex Parallelism single loop technique is used for recovering the original message.

IV. MODIFIED PARALLEL PREFIX CI- CSK ADDER

In the modified structure the middle stages of CI-CSKA is replaced by parallel prefix adder.Fig 1 describes the working of parallel prefix adder.There are mainly three stages in a PPA.The stages are preprocessing,parallel prefix network and post processing.the stages are discussed below.

A. Preprocessing Stage

In the preprocessing stage it generate propagation and generation signals using the given input bits.

B. Parallel prefix Network

The output of the pre processing stage is given to the next stage for generating carry bits.The parallel prefix network uses Brent kung adder[5].The pecualirty of this particular adder is that its fan out is very less and also wire length is less.it is mainly consists of three logic cells called black cell, gray cell and buffer cell.The black cell produces the group propagate and group generate.group propagate means AND gate and group generate means AND OR gate.Gray cell produces only the group generate and it is equals to carry output.

C. Post processing stage

The carry bit produced by the previous stage is given to next stage for finding the final sum results.

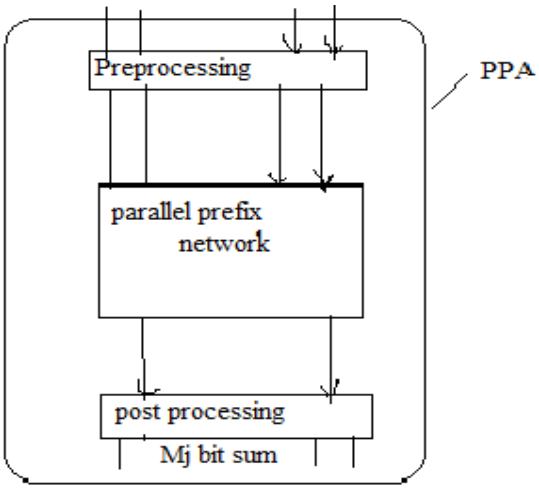

Fig 1. Working of PPA

D. Structure of parallel prefix CICSKA

The Structure of parallel prefix CICSKA consists of RCA block, incrementation block, skip logic and parallel prefix network.The incrementation block is just like an half adder.So by using the parallel prefix network in middle stages we can reduce the number of RCA block .The PPA structure find out the carry fastly increases the speed of the operation.The propagation signal from the PPA is used in skip logic to check whether the carry should be skipped or not.

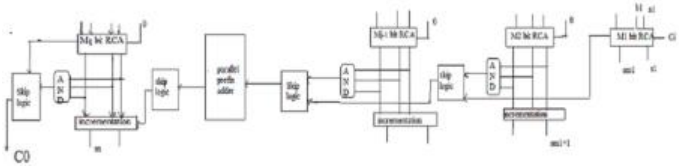

Fig.2 Structure of parallel prefix CICSKA

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V.SIMULATION RESULTS

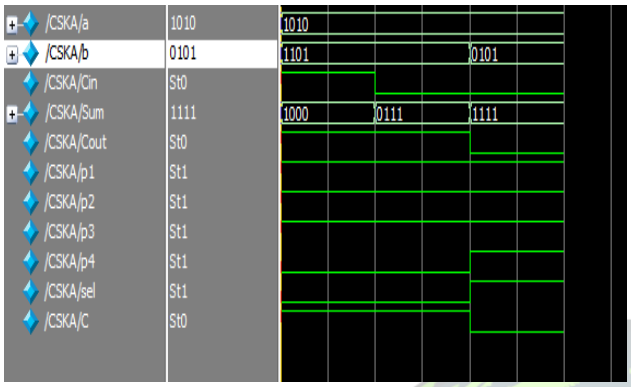

Fig.3 Conventional structure

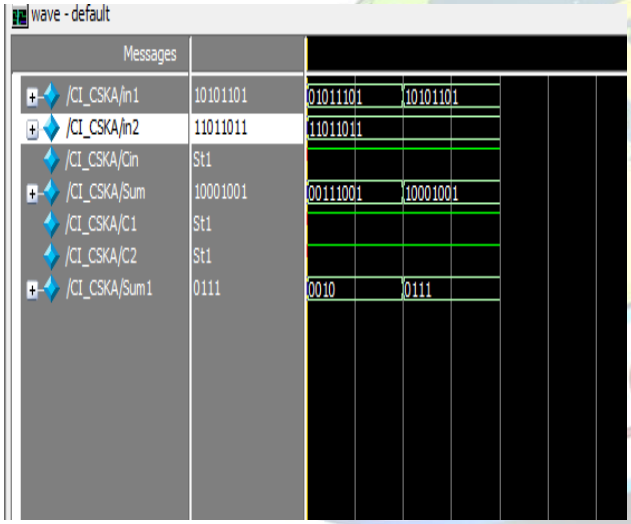

Fig.4 Incrementation Block wave form

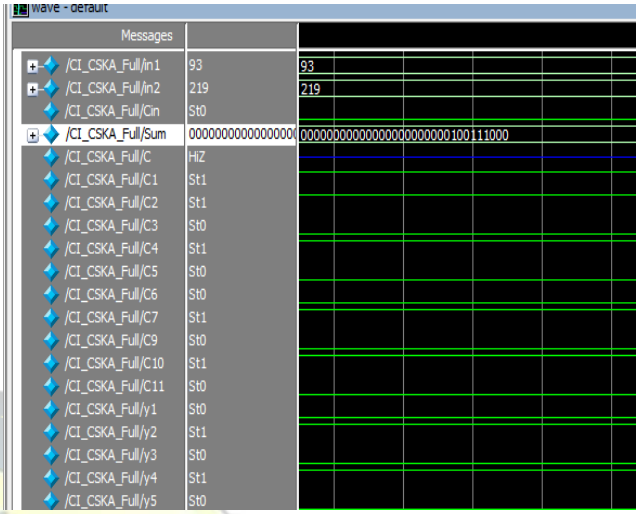

Fig.5 waveform of parallel prefix CI-CSKA

VI .CONCLUSION

In this paper a parallel prefix CI CSK adder structure was proposed.The advantage of this structure is that reduces the number of stages ,delays and the slack time.Prefix network is done by using the Brent kung adder which have lowest fan out.Using the parallel prefix structure we can generate carry fastly.High speed and energy efficient carry skip can be obtained by using this modified parallel prefix CI-CSK adder.

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